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Trace Cache Sampling Filter

Michael Behar, Avinoam Kolodny, Avi Mendelson

Abstract—**This paper presents a new technique for efficient usage of small trace caches. A trace cache can significantly increase the performance of wide out-of-order processors, but to be effective, the size of the trace cache should be large.**

Power and timing considerations indicate that a small trace cache is desirable, with special mechanisms to increase its effectiveness despite the limited size. Hence several authors have proposed various filtering methods to select "good traces" for keeping in the trace cache, from among the general population of traces.

This paper presents a new filtering technique, which is based on sampling. Our new technique suggests that instead of building all the traces and trying to select the good ones among them, it is more efficient to make a preliminary selection of traces. This selection is based on a random sampling approach.

We show that the Sampling Filter improves trace cache and overall system performance, while reducing power dissipation. The Sampling Filter reduces admission of traces that are not used prior to their eviction from the cache, and prolongs the percentage of time a trace is in its live phase during its stay in the cache. Moreover, the Sampling Filter reduces duplication between the trace cache and the instruction cache and thus reduces the overall misses in the first level of cache hierarchy.

Index Terms—**Trace cache, Filtering, Performance, and Power.**

1 Introduction

The effectiveness of a single threaded out-of-order processor is strongly dependent on the average number of useful instructions it can fetch in every cycle. Trace caches are very effective in serving this goal by storing instructions in their dynamic order rather than in their static order [10] [15] [16]. Thus, a trace cache has two major merits: it contains instructions from different basic blocks that would normally require several accesses to the instruction cache in order to be fetched, and it contains only useful instructions (contrary to an instruction cache line that is fetched but might include instructions that the processor doesn't require). The trace cache was found to be very effective if size and power are not limited. However, relatively small caches which are practical in term of access time and power consumption, are very vulnerable in terms of memory efficiency, because of several problems [11]: the same basic blocks can appear in different traces (duplication), some traces don't contain the maximum number of instructions (fragmentation), and the requested block might reside inside a trace and thus become inaccessible (Indexability). Thus, the key for efficient usage of relatively small trace caches is either to change the way the trace is constructed; i.e., the use of basic block traces [1], or to keep only the most valuable traces inside the cache and thus avoid their trashing by less valuable traces. This work will focus on the second option since the logic required to construct the traces out of a block-based cache is very costly in term of power.

Filtering (selective admission of incoming traces to the cache) has already been proposed as a way to increase the usefulness of a limited size trace cache. In [12] it was proposed to store only traces containing taken branches, which cannot be fetched in one access from the instruction cache. In [13] it was proposed to filter traces based on their usage. The trace cache is divided into two blocks: the Filter trace Cache (FTC) and the Main Trace Cache (MTC). All traces are written to the FTC, but only traces that have been proven to be "useful" are inserted to the MTC. The success of this filtering method is based on the important observation presented there [13], that most traces that are built and inserted to the trace cache are rarely used before eviction, and that most of the instructions the processor executes come from a small set of traces ("hot traces"). In [8] it was proposed to use profiling in order to filter out traces that are less frequent and show little time locality.

This paper presents a new class of trace filtering techniques, which is based on statistical sampling of traces. This class of filters aims to improve the quality of the traces residing in a small trace cache, while reducing the power dissipation needed for maintaining the filter's bookkeeping. The paper presents and analyzes the performance and the power of a basic Sampling Filter (SF) and an enhanced version of it, and compares its performance and power with a regular trace cache and with the FTC-MTC organization.

The rest of the paper is organized as follows: In Section 2 the simulation environment and the characterization of traces are discussed; Section 3 describes the sampling filter architecture and compares it with the regular trace cache and with the FTC-MTC organization. In Section 4 the usage of the Sampling Filter with the FTC-MTC organization is demonstrated and Section 5 concludes and proposes related ideas for future studies.

2 Simulation Environment and Basic Observations

This section presents the simulation environment we used, and some of the basic observations that our new proposed technique are based upon.

2.1 The simulation framework

The performance numbers presented below are based on an extended version of the sim-outorder simulator from the SimpleScalar tools set 3.0d [1] that was augmented with a detailed model of the trace cache that includes the impact of wrong path prediction and recovery, along with the simulation of the proposed filter mechanism and with a next trace predictor [6]. The power numbers presented in this paper were computed by an extended version of the Wattch [1] simulator

(which is based on Simple scalar) and by Cacti [17] that was used to estimate the power of new structures such as the trace cache, and for examining the impact of power and timing on caches with different configurations. The modeling of the leakage power in Wattch assumes that it always consumes 10% of the maximal dynamic power. In this work, since we assume relatively small structures of the trace cache, we saw that the leakage has only minor impact on the overall power of the chip and so we use the same method as in Wattch.

The structure of the traces within the trace cache we use for our model is similar to other works; i.e., a trace can contain up to 16 instructions and up to 4 branches, a trace is terminated also if it reaches indirect jumps, indirect branches, procedure-calls, return instructions and interrupts. Our traces are composed of basic blocks and we don't allow traces to be truncated unless a single basic block is larger than the trace capacity (in our framework: 16 instructions). We allow loop unrolling and don't terminate a trace upon a backward branch. This allows traces to contain enough instructions to have an advantage over the regular fetch mechanism and yet not increase the number of unique traces too much. In this paper we focus on two sizes of the trace cache: one that contains 32 traces, and another that contains 64 traces, both organized as 4-way set-associative. Our trace build mechanism allows traces beginning at the same address, but with multiple paths, to coexist in the trace cache. In this case, it is up to the trace predictor to decide which of the traces to select. The work assumes a trace cache with a backing instruction cache, which are accessed in parallel as was described in [16].

The configuration of the baseline machine is presented in Table 2.1. We chose an 8-way machine as a baseline since it can take advantage of the improvement in instruction supply and still be power efficient.

WE USED 10 BENCHMARKS (SEE

Table 2.2) from the SPEC2000 Benchmark Suite [4] to evaluate our work. We skipped the first 500M instructions and simulated another billion instructions in all our experiments except perlbmk that was ended after 880M instructions.

2.2 Basic observations

We start this section by presenting basic characterization of the utilization of each trace in the trace cache, and characterization of the utilization of the trace cache itself. Trace Utilization (TU) is defined to be the number of times the system finds the trace in the trace cache per a trace build. Please note this definition does not require that the traces will be unique; i.e., if a trace is replaced and built again, we count it as two different traces. Also, the length of the trace does not affect the utilization of the trace.

A trace cache with a high TCU is assumed to be power and performance efficient. For a 32-traces trace cache the average TCU is five. Moreover, five out of the ten benchmarks we examined have a TCU smaller than 2. Therefore, the power invested in writing traces to the trace cache is very poorly used.

TABLE 2.1 ARCH SETTINGS OF THE SIMULATED MODEL.

Execution engine	
Decode, Issue, Commit width	8
Functional units	Integer ALU's: 8 4 Mult/Div. Floating point ALU's: 8 4 Mult/Div.
Instruction fetch queue size	32
Register update unit (RUU)	128
LSQ	64
Memory	
L1 Data Cache	64KB 8-ways LRU, 64B blocks. 2-cycle latency.
L1 Instruction Cache	8KB 4-way, LRU, 32B block, 2-cycle latency
Trace cache	2KB (32 traces)/4KB (64 traces) 4-way, LRU, 2-cycle latency
L2 Unified cache	1MB 8-ways, 64B blocks.LRU, 10-cycle latency
Memory	First chunk: 128 cycles
TLB	30 cycles miss penalty
Branch predictor	
Predictor	Bimod 4k-entery
RAS	32
BTB	2K-entery, 4-way
Next trace pred	4K-entery

TABLE 2.2 BENCHMARKS LIST.

Benchmark	Input	Suite
164.gzip	input.graphic	INT
175.vpr	net.in arch.in place.in	INT
176.gcc	166.i	INT
197.parser	2.1.dict –batch ref.in	INT
253.perlbmk	makerand.pl	INT
255.vortex	lendian1.raw	INT
256.bzip	input.graphic	INT
177.mesa	mesa.in mesa.ppm	FP
183.equacke	inp.in	FP
168.wupsize	wupwise.in	FP

$$TCU = \frac{\sum hits}{\sum writes}. \quad (1)$$

The replacement rate (RR) of traces in the traces cache is defined by:

$$RR = \frac{\sum replacements}{\sum accesses}. \quad (2)$$

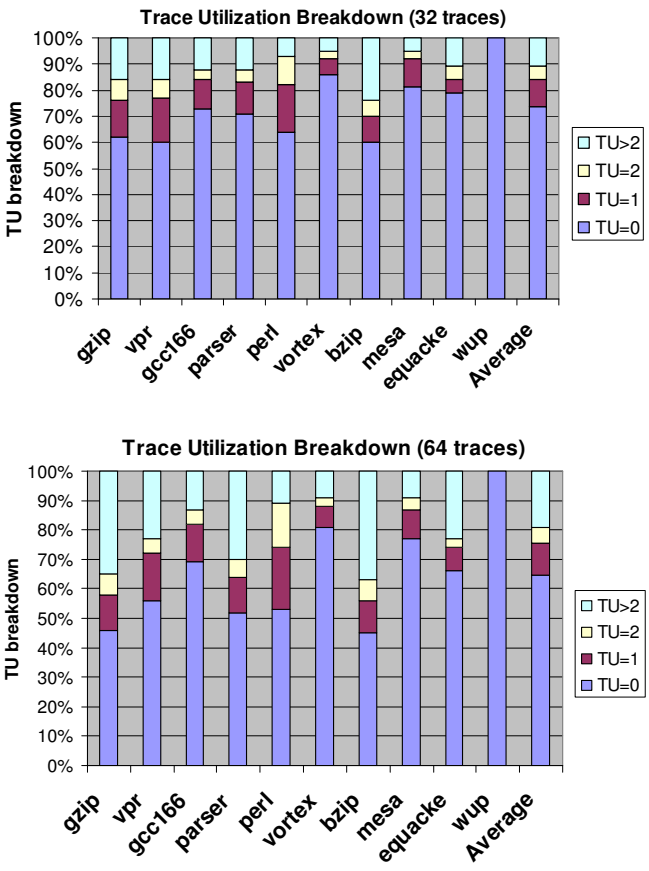

Figure 2.1 Trace utilization breakdown for a 32-traces trace cache (top figure) and for a 64-traces trace cache (bottom figure). In both configurations the majority of traces that are written to the trace cache are not used prior their eviction from it.

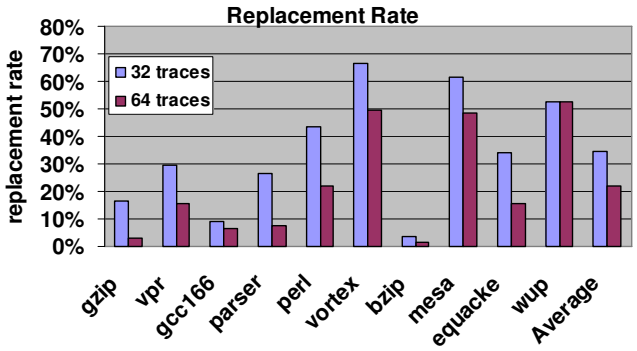

Figure 2.2 Trace cache replacement rate.

Figure 2.2 shows the replacement rate of a 32-traces and 64-trcaes trace cache. It is clear from the figure that for some applications, even a small trace cache can contain the whole program, but for other applications such a trace cache is too small. On average, the replacement rate is high (34% and 22% for a 32-traces and 64-traces caches respectively).

The above observations indicate that for a limited area trace cache, traces are replaced too frequently by less effective traces and cause the entire trace cache mechanism to be ineffective in terms of performance and power. Therefore, it is critical to filter "good" traces out of the general population of traces.

3 THE SAMPLING FILTER

Unlike other proposed filtering techniques that try to keep track of all traces in the program in order to classify them as "hot traces" (that need to be kept) or "cold traces" (that can be discarded), the new proposed technique uses a statistical approach. By using statistical methods, we suggest to randomly select traces, which are candidates for storing in the trace cache. Please note that by doing so, we do not preclude any other filtering techniques, which can be applied on the chosen subset of the traces.

The structure of a system that supports the basic sampling algorithm is shown in Figure 3.1. On top of a trace cache system as described in [16] we add a sampling capability that chooses periodically, for example every X builds, to save a trace. Traces that are not sampled (selected) are discarded. The sampling rate is the rate at which traces are sampled i.e. if every tenth trace is inserted to the trace cache, the sampling rate is 1/10. This filtering mechanism requires minimal hardware and can be easily implemented.

In order to establish the new proposed technique effectiveness, the next subsection provides some performance (IPC) and power efficiency (ED^2) simulation measurements as well as trace cache behavior (hit rate and coverage). Next we will extend the discussion in order to understand why it works and how it can be further improved.

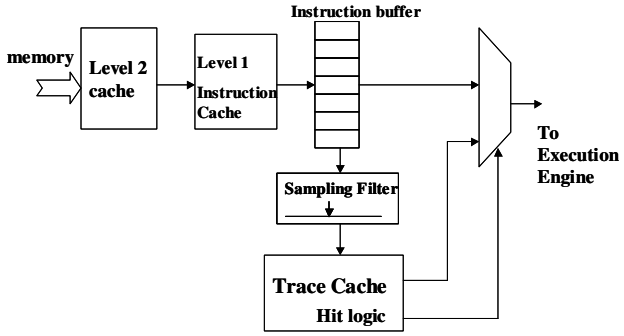

Figure 3.1 The Sampling Filter system.

3.1 The Impact of the Sampling filter

In this section we compare several fetch engine configurations. The different configurations and area budget are summarized in Table 3.1. The regular trace cache (CTC32) and the Sampling Filter (SF32) machines all have a 8KB backing instruction cache and a 2KB trace cache size. The FTC-MTC organization has also an 8KB backing instruction cache and a 2KB total trace cache that is divided equally between the FTC and the MTC. The SF32 uses a constant sampling rate of 1/20 for all the benchmarks.

Figure 3.2 shows the IPC improvement of these fetch

engines over a machine without a trace cache, which has an 8KB instruction cache only (I8KB). Doubling the Instruction cache to a 16KB cache (I16KB) improves the IPC by 10%, while the regular trace cache (CTC32) improves performance by 10.7%. The FTC-MTC achieves 12.4% improvement while the Sampling Filter (SF32) achieves 17.5% improvement. This demonstrates that the combination of a small trace cache (total area of 10KB) and sampling technique can outperform a larger instruction cache (16KB) and the other trace cache organizations occupying the same area.

TABLE 3.1 FETCH ENGINES CONFIGURATIONS

CONFIGURATION NAME	CONFIGURATION DESCRIPTION	TOTAL AREA
I8KB	Instruction cache	8KB
I16KB	Instruction cache	16KB
CTC32	Concurrent trace cache	10KB
FTC-MTC	Filter trace cache + Main trace cache	10KB
SF32	Concurrent trace cache with a sampling filter	10KB

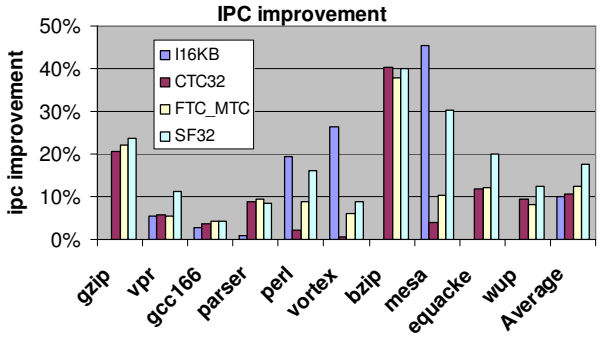

Figure 3.2 IPC improvement over a regular 8KB instruction cache.

Figure 3.3 shows the reduction in energy delay squared (ED^2) of several fetch engines compared with a regular 8KB instruction cache. The 16KB instruction cache achieves a reduction of 13.6% in ED^2. The trace cache and the FTC-MTC organization achieve 15.8% and 18.9% reduction in ED^2 respectively, while the Sampling Filter achieves a 27.4% reduction in ED^2. This indicates that the sampling filter is the most performance-power efficient among the compared alternatives.

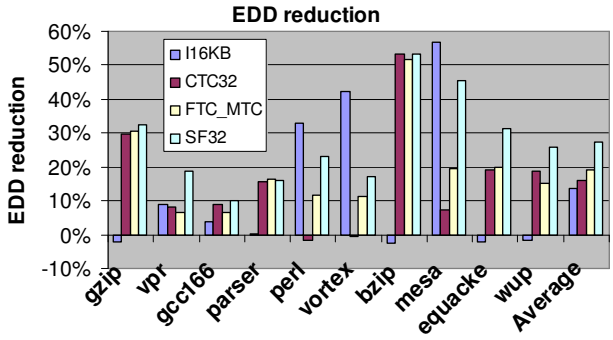

Figure 3.3 ED^2 reduction over a regular 8KB Instruction cache. The Sampling Filter proves to be the most performance-power efficient out of all the configurations.

The impact of sampling on the trace cache behavior is presented in Figure 3.4. The coverage (the percentage of instructions originated from the trace cache) of the Sampling Filter configuration compared with the regular trace cache increases from 56.5% to 66.3%. The hit rate of the Sampling Filter configuration increases from 66% to 72.6%.

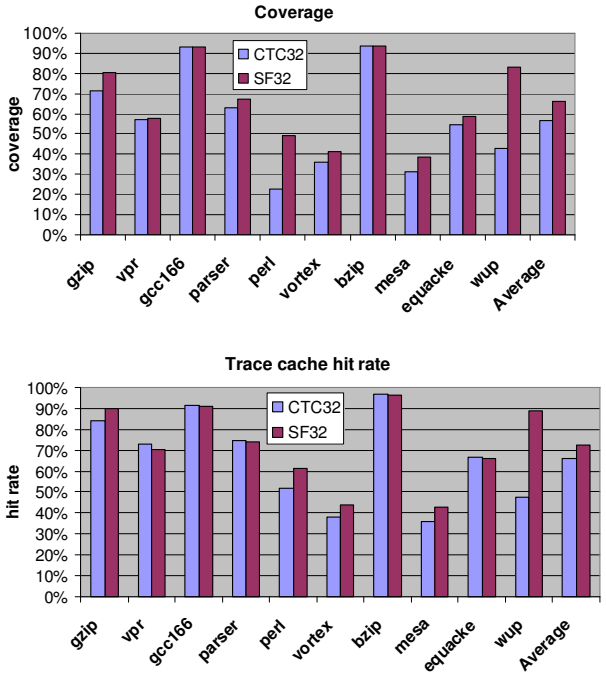

Figure 3.4 Trace cache coverage (top figure) and hit rate (bottom figure) of a regular trace cache (CTC32) and the sampling filter organization (SF32).

3.2 Why it works

The reason that our new technique works so well is a combination of two effects: the reduction of pressure of new coming traces on the small trace cache, together with the impact of the LRU mechanism. As was published in some researches in the past, it is known that most of the instructions a trace cache based processor executes come from a relatively small number of traces ("hot traces"). These traces, regardless of the random selection, will be selected eventually, and will

be placed in the trace cache. The main impact of the sampling filter is then, on the "cold traces". In section 2 it has been shown that the majority of writes are of "cold traces" with zero TU rate. The filter reduces the number of "cold traces" writes. This reduces the pressure on the small trace cache and enables the LRU mechanism to better capture the "hot traces", so "cold traces" that happened to enter the cache can be identified as such, and be replaced.

In order to justify the above claims, we present a new set of experiments. Figure 3.5 shows the impact of using the basic sampling algorithm on the trace utilization (TU), and in particular we focus on the percentage of traces that have TU=0. We can observe that the sampling technique reduces the population of these traces dramatically from 73.8% in the non-filtered system to 25.6% in the sampling filter system. The impact of such reduction in the "useless traces" is twofold: it saves a lot of wasted power and it prevents cache pollution by inefficient traces.

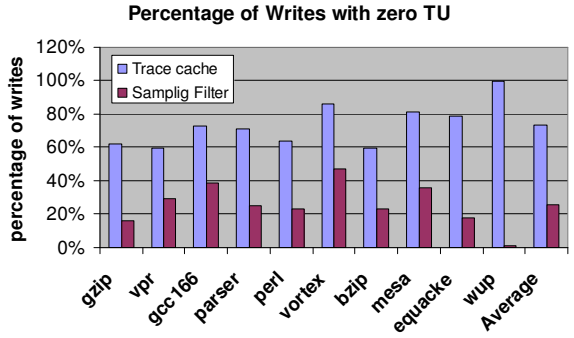

Figure 3.5 Percentage of writes with zero TU.

An important indicator for the quality of a trace is the proportion between its "live" time and its "decay" time as was defined in [13] [7]. A "live" time of a trace is measured from the time it was saved in the trace cache till the last time it was used. The "decay" time of a trace is measured from the last time it was used, until its eviction from the trace cache. Since the decay time is considered to be a waste of resources, we try to reduce it. Figure 3.6 shows the impact of the sampling technique on the lifetime of traces. While in the regular trace cache the average "live" time of a trace is only 32%, after applying our new sampling technique, about 75% of the time, a trace is "live". For small trace caches the utilization of the area is very important and so it can explain why we see a vast improvement in performance due to our technique.

So far we saw that the sampling technique improves both the trace utilization and the "live" time of traces within the cache. Table 3.2 shows that the proposed sampling technique also improves the overall utilization of the entire trace cache (TCU). This result has significance of its own. Several works have proposed to use hardware to optimize frequent code on the fly [14] [9]. By increasing the TCU, the sampling filter ensures that optimized code will be reused many times prior to its replacement. Therefore, costly hardware optimization can be applied on traces that are inserted to the trace cache because the number of insertions is low and the utilization rate is high. The trace cache utilization rate increased 21.2 times for a Sampling Filter configuration over the regular trace cache (see Table 3.2).

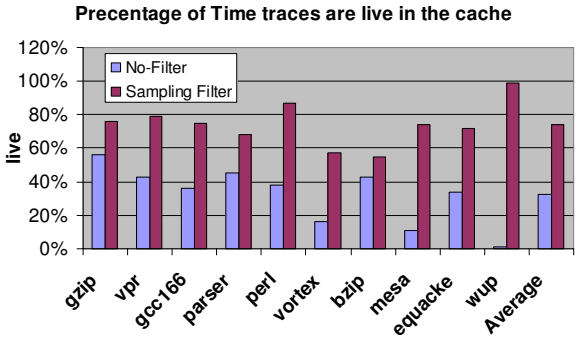

Figure 3.6 Percentage of time traces are live in the cache.

TABLE 3.2 TCU OF A TRACE CACHE, A SF SYSTEM AND THEIR RATIO.

BENCHMARK	REGULAR TRACE CACHE	SAMPLING FILTER	RATIO
gzip	5.13	160.69	31.3
vpr	2.45	41.65	17.0
gcc166	10.37	191.43	18.5
parser	2.84	51.13	18.0
perl	1.19	36.84	31.0
vortex	0.57	14.4	25.3
bzip	28.1	435	15.5
mesa	0.59	15.02	25.5
equacke	1.97	39.77	20.2
wup	0.9	162.39	180.4
Average	5	115	21.2

3.3 Power considerations in Sampling Filter

So far we focused on the performance aspects of the Sampling Filter technique. This subsection extends the discussion to power considerations and shows that the sampling technique is also advantageous in terms of power. The main reasons for that are the significant reduction in power that is used to write inefficient traces to the cache, and the better utilization of the trace cache that leads to fewer builds from the instruction cache. In Table 3.3 the number of writes per 100 committed instructions is presented for a regular trace cache and a Sampling Filter organization. On average, the sampling filter organization has 29 times less writes to the cache than a regular trace cache.

TABLE 3.3 NUMBER OF WRITES PER 100 COMMITTED INSTRUCTIONS IN A REGULAR TRACE CACHE , SF SYSTEM AND THEIR RATIO.

BENCHMARK	REGULAR TRACE CACHE	SAMPLING FILTER	RATIO
Gzip	2.25	0.08	28.14
vpr	3.47	0.18	18.82
gcc166	0.71	0.04	18.79
parser	3.22	0.18	18.28
perl	0.79	0.03	26.51
vortex	5.76	0.26	22.19
bzip	0.44	0.03	15.73
mesa	5.37	0.24	22.56
equacke	3.58	0.16	22.74
wup	3.48	0.04	96.00
Average	2.91	0.12	28.98

Figure 3.7 shows the fetch stage power of three equal area trace configurations: a regular trace cache, the FTC-MTC organization and the Sampling Filter organization. The FTC-MTC filter increases the fetch stage power by 14% as it involves accessing two cache structures in parallel (the FTC and the MTC) and doesn't reduce the number of builds significantly. On the other hand, the Sampling Filter reduces the fetch stage power by 10% over a regular trace cache, as it reduces the number of builds.

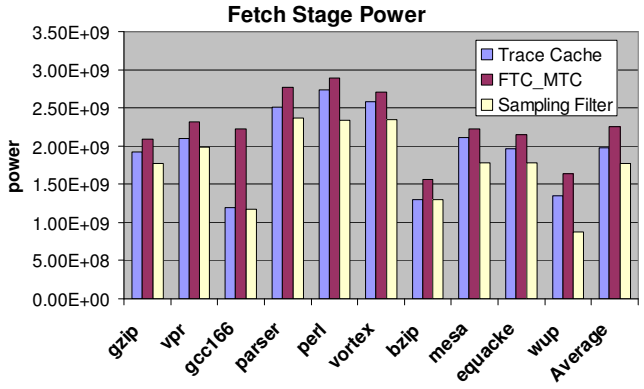

Figure 3.7 Fetch stage power of the trace cache, the FTC-MTC organization and the SF organization.

3.4 Trace and Instruction cache decoupling

The purpose of the sampling filter is to reduce the percentage of low utilization rate traces. By reducing the number of writes to the trace cache the sampling filter also accomplishes a reduction in the overall miss rate at the Level 1 caches hierarchy (Trace cache and Instruction cache together). The backing instruction cache is important because it provides the instructions to build a trace upon a trace cache miss. Accessing the Level 2 cache to build traces would reduce the performance because of the L2 longer access time. After the trace is built the code is present in the trace cache as well as in the instruction cache. Thus, the code is duplicated and the Level 1 memory is not used efficiently. If the trace is repeatedly rebuilt then it will continue to be duplicated in both the trace cache and the instruction cache. The ability of the Level 1 backing instruction cache to provide a high percentage of the trace misses is essential for maintaining a high instruction bandwidth. The sampling filter decouples the Trace Cache and the Instruction Cache by prolonging the lifetime of traces in the trace cache. At first, the basic blocks of a trace that was inserted to the trace cache are present in the instruction cache as well. But, those basic blocks are gradually replaced by the LRU replacement policy of the instruction cache, because the trace cache holds and serves them repeatedly over time. Consequently, duplication among the caches is reduced, and the overall instruction supply out of L1 caches is improved. In order to demonstrate the decoupling effect, we conduct a new set of experiments on a system with a small 4KB backing instruction cache. Figure 3.8 shows the instruction cache miss rate for various sampling rates. The miss rate is presented only for benchmarks that have an instruction cache miss rate higher than 0.5%. As the sampling rate decreases the decoupling effect is stronger and so the instruction cache miss rate decreases.

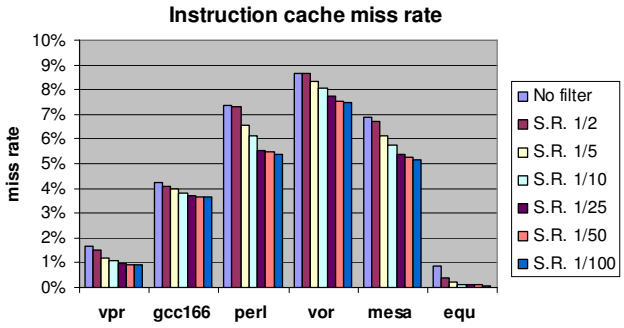

Figure 3.8 Instruction cache miss rate of benchmarks with a miss rate higher than 0.5% for various sampling rates (S.R.)

The impact on the IPC is presented in Figure 3.9. The Average IPC over all the benchmarks is improved by 12.1% for a sampling rate of 1/100. The sampling filter improves the perlbmk benchmark by 43% over the "regular" trace cache (sampling rate of 1/100) as the Level 1 cache hierarchy is able to supply many more instructions.

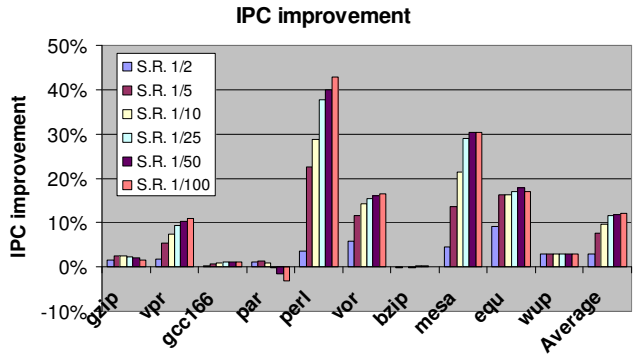

Figure 3.9 IPC improvement over a regular trace cache for various sampling rates (S.R.).

4 COMBINING THE SAMPLING FILTER WITH THE FTC-MTC ORGANIZATION

The sampling filter is orthogonal to the FTC-MTC principle, hence the two can be combined. By placing the sampling filter in front of the FTC cache (see Figure 4.1), the utilization rate of traces in the FTC can be improved. Moreover, by reducing the number of writes to the FTC it can better monitor the behavior of traces. The decision whether to discard the trace or store it in the MTC is taken after a longer period and thus the observation better reflects the nature of the trace. Figure 4.2 and Figure 4.3 show the improvement in IPC and the reduction in ED^2 of several filter organizations over a regular trace cache. The combination of the sampling filter with the FTC-MTC organization improves the IPC by 9.8% and the ED^2 by 20.2% while the sampling filter improves the IPC and ED^2 only by 6.46% and by 14.9%, respectively. The combination of the sampling filter with the FTC-MTC organization outperforms both the sampling filter and the FTC-MTC organization, applied separately.

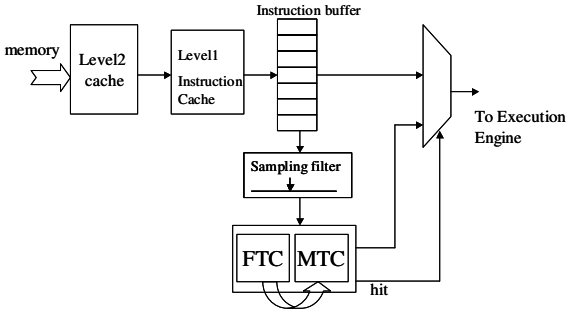

Figure 4.1 Sampling Filter with FTC-MTC.

The Hit rate and Coverage of different trace cache organizations are presented in Figure 4.4 and Figure 4.5 respectively. The combination of the sampling filter with the FTC-MTC organization increases the average hit rate by 17% over a regular trace cache (from 66% to 77.2%) while the sampling filter increases the hit rate only by 9.9% (from 66% to 72.5%). The coverage shows the same tendency, the coverage of the sampling filter is improved by 17.2% (from 56.5% to 66.3%) and the combination of the sampling filter and FTC-MTC organization improves the coverage by 24.2% (from 56.5% to 70.2%) over a regular trace cache.

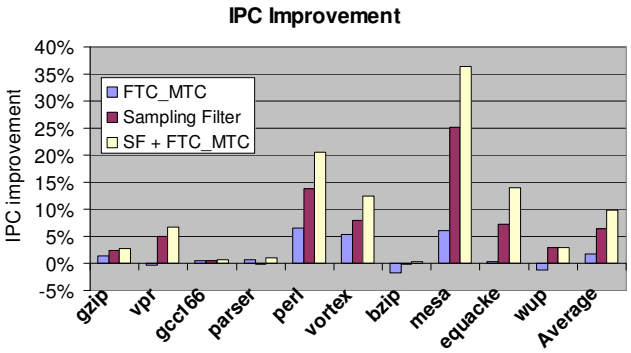

Figure 4.2 IPC improvement of different sampling techniques over a regular trace cache.

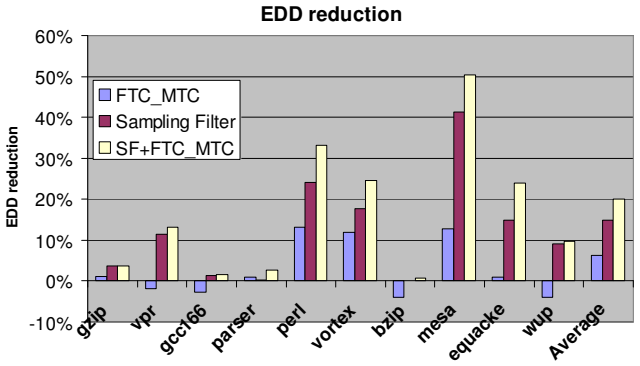

Figure 4.3 ED^2 reduction of different sampling techniques over a regular trace cache.

These results indicate that the ability of the FTC-MTC organization to capture the "hot traces" in the MTC is well complemented by the ability of the Sampling Filter to reduce the number of "cold traces" writes.

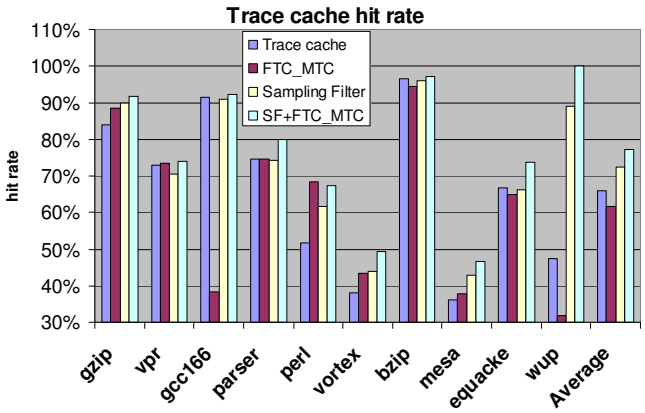

Figure 4.4 Hit rate of different trace caches configurations.

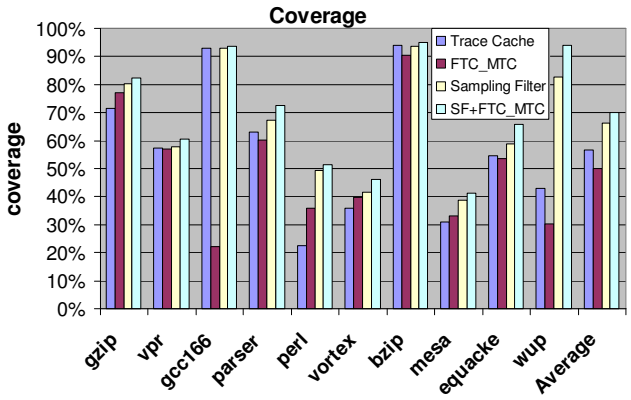

Figure 4.5 Coverage of different trace caches configurations.

5 DISCUSSION AND CONCLUSION

In this paper we investigated the impact of filtering on small trace caches and proposed a novel filter: the sampling filter. Small trace caches are efficient in terms of power and access time but suffer from low utilization of the memory space. In order to increase the effectiveness of small trace caches, filtering mechanisms can be applied. The sampling filter is a novel filter that is based on a random sampling approach. Rather than inserting each trace to the trace cache and then monitoring its behavior, the sampling filter reduces the number of writes to the trace cache. It exploits the fact that most writes to the trace cache are of traces that are not used prior their eviction. The traces that are executed many times from the trace cache (and contribute most of the committed instructions) are captured quickly by the sampling filter and maintained in the cache more efficiently by the LRU mechanism.

This paper showed that the sampling filter improves the trace cache behavior in terms of coverage and hit rate while the fetch stage power is reduced. The power of the fetch stage is reduced as the number of writes to the trace cache can be dramatically reduced while the number of hits in the trace cache increases. The coverage improvement can be especially beneficial for systems that store instructions in the trace cache after some processing, e.g. the Pentium 4 [5]. From a system perspective, the IPC and ED^2 are improved as well.

The sampling filter also improves the utilization of the Level 1 caches hierarchy (instructions cache and trace cache together) by decoupling the instruction cache and the trace cache.

The combination of the FTC-MTC organization with the sampling filter yields better results than each of the filters alone. This leads us to believe that the sampling filter random selection can be replaced by a more intelligent selection. Future research will focus on implementing such an intelligent selection, based on trace utilization, while maintaining the filter power efficiency. We also intend to present an adaptive mechanism to optimize the sampling rate for each program and trace cache size dynamically.

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