

Unified Logical Effort - A Method for Delay Evaluation and Minimization in Logic Paths with *RC* Interconnect

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Abstract - A model for delay evaluation and minimization in logic paths with gates and *RC* wires is presented. The method, *Unified Logical Effort* (ULE), provides closed-form conditions for timing optimization while overcoming the breakdown of standard logical effort (LE) rules in the presence of interconnect. The ULE delay model and optimization unifies the problems of gate sizing and repeater insertion: In cases of negligible interconnect, the ULE method converges to standard LE optimization yielding tapered gate sizes. In the case of long wires, the solution converges towards uniform optimal sizing of the gates as in repeater insertion methodologies. The technique is applied to various logic path examples, while investigating the influence of wire length, gate type, and technology. Techniques for combining the ULE method with existing heuristics of buffering and repeater insertion are also proposed.

I. INTRODUCTION

Timing modeling and optimization is one of the main issues in high complexity circuit design. The method of logical effort (LE) was first proposed by Sutherland *et al.* [1] for fast evaluation and optimization of delay in logic paths (see Fig. 1a). The technique has since been adopted as a basis for many CAD tools, thanks to the simplicity of LE. The LE method benefits from an uncomplicated and intuitive delay model and closed-form optimization conditions. The optimization rule of logical effort, however, only addresses logic gates and does not consider on-chip wires. As VLSI circuits continue to scale, the contribution of wires to the delay increases and cannot be neglected. This characteristic occurs not only with respect to long wires interconnecting separate modules but also to inside of logic modules where the delays introduced by the wires interconnecting closely coupled gates approach and even exceed gate delays. The handy LE rule that the delay is minimum when the effort of each stage is equal breaks down, because interconnect has fixed capacitances which do not correlate with the characteristics of the gates (see Fig. 1b). This behavior is described by the authors of the LE method as “one of the most dissatisfying limitations of logical effort” [2].

The primary objective of this work is to develop a simple method for optimizing timing in logic paths containing both gates and interconnect. Currently, timing optimization is typically treated separately in two cases: (a) logic gates without wires (using the standard LE method), (b) long wires without logic (using

repeater insertion). In this paper, the *Unified Logical Effort* (ULE) method is presented for delay evaluation and optimization in logic paths with general gates and *RC* wires. ULE treats a broad scope of design problems with a single analytic model, while combining both logic and interconnect delay optimization. ULE reduces in particular cases to the well-known optimal gate size tapering [1] for gates without wires, and to optimal wire segmenting with repeaters [3].

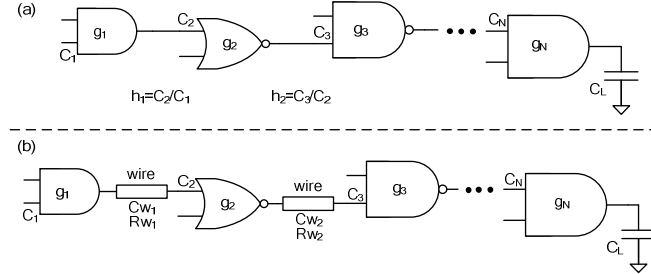


Fig. 1. Cascaded string of logic gates. (a) Logical effort optimization for gates without wires is based on equal stage efforts $g_1 h_1 = g_2 h_2$ etc. , (b) in case of gates with wires, the rule of equal effort breaks down because of fixed wire parameters.

The paper is composed of the following sections. Related works are surveyed and discussed in Section III. The Unified Logical Effort model is developed in Section III. Timing optimization based on the ULE model referring to resistive and capacitive wires is presented in Section IV. A simple and fast method for determining the optimal gate size is also demonstrated. Examples of ULE optimization are presented in Section V. Convergence of the model to existing optimization techniques is shown for specific cases. Finally, a summary of the paper as well as discussion and future work are provided in Section VII.

II. RELATED WORKS

Research has been previously carried out to increase the accuracy of the logical effort model by considering I/O coupling and input ramp effects [15], as well as internodal charge and deep submicrometer effects [9]. While extending the LE method for increased accuracy of logic gate delays, these papers do not address the issue of interconnect. Some publications proposed an extension of logical effort to address the delay of the wires while using the term 'interconnect effort'. Logical effort optimization is performed in [13] on logic blocks driving interconnect with uniform and non-uniform repeaters. That work, however, does not include closed-form analytic expressions for delay estimation and optimization.

Traditional timing optimization procedures have been developed assuming capacitive interconnect [4],[5], [6]. This research focuses on optimal tapering of buffers driving the interconnect. In [7], [8], the wire capacitance between the gates is treated as correlated to the gate size, resulting in fixed tapering factors similar to the logical effort model. In [6], local interconnect capacitances are considered as independent of the gate size and the optimization is developed heuristically based on constant capacitance-to-current ratio tapering. In order to handle resistive interconnect, post-routing design steps have been added, involving wire segmentation and repeater insertion. These optimization techniques include equal sizing and spacing of the repeaters [3], as well as tapering the repeater size and wire segments [13]. All of these techniques for timing optimization in interconnect have been developed regardless of the logical

effort model, and only focus on inverters as buffers and repeaters over long interconnects, rather than on general logic paths with wire segments.

The LE delay expression is used for optimal wire segmentation by placing general logic gates rather than repeaters in [11] and [14]. The model in [11] uses a concept of resistive effort which is added to the logical effort expression. The model provides a specific optimization technique of logic gates spaced along interconnect. An extension of logical effort is also used in [14] for developing an optimization methodology utilizing logic gates as repeaters. The delay expressions in these papers are only used as a basis for partitioning a long wire by logic gates, and have not been analyzed for the general case of a logic path with interconnects.

III. EXTENSION OF THE LOGICAL EFFORT MODEL TO LOGIC GATES WITH WIRES

The logical effort model is modified here to include the interconnect delay. This change is achieved by extending the gate logical effort delay by the wire delay, establishing a *Unified Logical Effort* (ULE) model. In this Section, components of ULE are derived for use in the following section in order to determine the conditions for delay optimization.

The combined circuit of logic gates with wires is shown in Fig. 2. The interconnect is represented by a π -model. Following [17], the Elmore delay model [1] is used to describe the wire segment delay. Note that the analytic approach described in this paper can also be successfully applied to other interconnect models, both lumped and distributed. The total combined delay expression is:

$$D_i = R_i \cdot (C_{p_i} + C_{w_i} + C_{i+1}) + R_{w_i} \cdot (0.5 \cdot C_{w_i} + C_{i+1}), \quad (1)$$

where C_{p_i} is the parasitic output capacitance of gate i , C_{w_i} and R_{w_i} are, respectively, the wire capacitance and resistance of segment i , and C_{i+1} is the input capacitance of gate $i+1$.

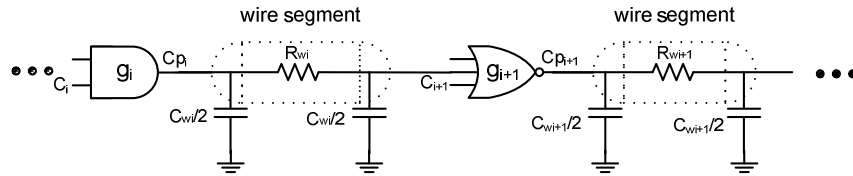


Fig. 2. Logic gates with interconnect load.

This expression is rewritten by introducing the delay of a minimum size inverter $\tau = R_0 \cdot C_0$, where R_0 and C_0 are the output resistance and input capacitance of the inverter, respectively

$$D_i = \tau \cdot \left[\frac{R_i}{R_0} \cdot \frac{(C_{w_i} + C_{i+1} + C_{p_i})}{C_0} + \frac{R_{w_i}}{R_0 \cdot C_0} \cdot (0.5 \cdot C_{w_i} + C_{i+1}) \right]. \quad (2)$$

The components in the delay expression are transformed to the form used in the logical effort (LE) model [1]. The delay of a logic gate is expressed in LE as a value d_i independent of the particular technology and normalized with respect to a minimum inverter delay τ :

$$D_i = \tau \cdot d_i = \tau \cdot (g_i \cdot h_i + p_i), \quad (3)$$

where $g_i = (R_i \cdot C_i) / (R_0 \cdot C_0)$ is the logical effort related to gate topology, $h_i = C_{i+1} / C_i$ is the electrical effort describing the driving capability, and $p_i = (R_i \cdot C_{p_i}) / (R_0 \cdot C_0)$ is the parasitic delay factor.

The expression of total stage delay, using LE terms, is

$$d_i = g_i \cdot \left(h_i + \frac{C_{w_i}}{C_i} \right) + \frac{R_{w_i} \cdot (0.5 \cdot C_{w_i} + C_{i+1})}{\tau} + p_i. \quad (4)$$

The *capacitive interconnect effort* h_w and the *resistive interconnect effort* p_w are defined as follows,

$$h_{w_i} = \frac{C_{w_i}}{C_i}, \quad p_{w_i} = \frac{R_{w_i} \cdot (0.5 \cdot C_{w_i} + C_{i+1})}{\tau}. \quad (5)$$

As shown in (5), h_w expresses the influence of interconnect capacitance on the electrical effort of the gate. The component p_w is the delay of the loaded wire in terms of the gate delay (τ). The component $(R_w \cdot 0.5 \cdot C_w) / \tau$ is technology specific.

The final expression of the ULE delay for a single stage is

$$d = g \cdot (h + h_w) + (p + p_w). \quad (6)$$

The ULE delay expression for an N stage logic path with RC wires is

$$d = \sum_{i=1}^N g_i \cdot (h_i + h_{w_i}) + (p_i + p_{w_i}). \quad (7)$$

Note that in the case of short wires, the resistance R_w of the wire may be neglected, eliminating p_w and leaving only the capacitive interconnect effort h_w in the expression. The extended delay expression of (4) reduces to the LE delay equation when no wires exist along the logic path.

IV. UNIFIED LOGICAL EFFORT OPTIMIZATION

In this section, the ULE method is developed for delay optimization of a general logic path with interconnect. The optimum conditions in terms of the electrical efforts are presented and analyzed for resistive and capacitive wires. Close-form expressions are derived for optimal gate sizing followed by a method for fast and simple calculation of optimal gate sizing along a logic path with wires.

As the first step in optimizing the ULE expression, a two-stage portion of a logic path with wires (as shown in Fig. 2) is considered. In this case, the ULE expression of the total delay is

$$d = g_i \cdot (h_i + h_{w_i}) + (p_i + p_{w_i}) + g_{i+1} \cdot (h_{i+1} + h_{w_{i+1}}) + (p_{i+1} + p_{w_{i+1}}), \quad (8)$$

where the electrical effort of each stage is $h_i = C_{i+1} / C_i$ and $h_{i+1} = C_{i+2} / C_{i+1}$. A plot of the delay as a function of the gate capacitance is illustrated in Fig. 3. The input capacitance is related to the driving ability

of the gate. The plot demonstrates an extreme point, where the optimal gate capacitances result in the minimum delay.

Substituting $C_{i+1} = h_i \cdot C_i$ into (8) in the presence of resistive interconnect, the delay can be expressed in terms of h_i

$$d = g_i \cdot \left(h_i + \frac{C_{w_i}}{C_i} \right) + p_i + \frac{R_{w_i} \cdot (0.5 \cdot C_{w_i} + h_i \cdot C_i)}{R_0 \cdot C_0} + g_{i+1} \cdot \left(\frac{C_{i+2} + C_{w_{i+1}}}{h_i \cdot C_i} \right) + p_{i+1} + p_{w_{i+1}}. \quad (9)$$

The optimal condition is determined by equating the derivative of the delay to zero

$$\frac{\partial d}{\partial h_i} = g_i + \frac{R_{w_i} \cdot C_i}{R_0 \cdot C_0} - g_{i+1} \cdot \left(\frac{C_{i+2} + C_{w_{i+1}}}{h_i^2 \cdot C_i} \right) = 0, \quad (10)$$

$$h_i = \sqrt{\frac{g_{i+1}}{g_i + \frac{R_{w_i} \cdot C_i}{R_0 \cdot C_0}} \cdot \left(\frac{C_{i+2}}{C_i} + \frac{C_{w_{i+1}}}{C_i} \right)}. \quad (11)$$

Substituting $C_{i+2}/C_i = h_i \cdot h_{i+1}$ and $C_{w_{i+1}}/C_i = h_i \cdot h_{w_{i+1}}$,

$$h_i = \sqrt{\frac{g_{i+1}}{g_i + \frac{R_{w_i} \cdot C_i}{R_0 \cdot C_0}} \cdot (h_i \cdot h_{i+1} + h_i \cdot h_{w_{i+1}})}. \quad (12)$$

The general condition of the electrical effort for minimal delay of logic stage i with RC interconnect is

$$\left(g_i + \frac{R_{w_i} \cdot C_i}{R_0 \cdot C_0} \right) \cdot h_i = g_{i+1} \cdot (h_{i+1} + h_{w_{i+1}}). \quad (13)$$

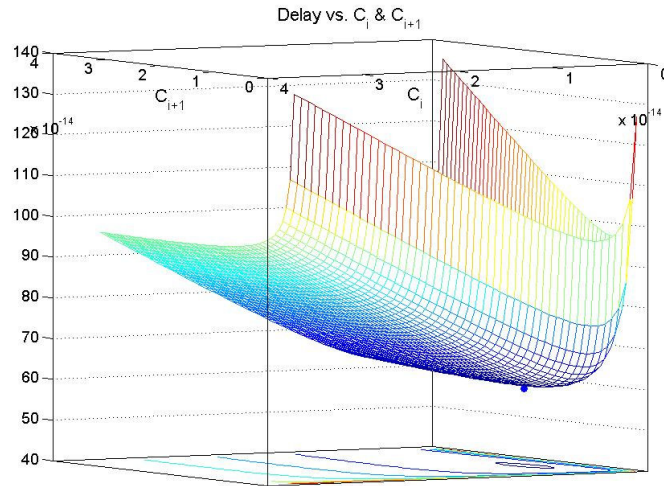


Fig. 3. Delay profile as a function of gate capacitance for 100 μm wires. The minimum delay can be used to determine the optimal gate size.

The second component $h_{w_{i+1}}$ is added to the electrical effort of gate $i+1$, expressing the increased capacitive load applied by wire segment $i+1$ to the gate. By applying the optimum condition to each pair of gates along the path, all interconnect components can be accounted for. Since (13) refers to the electrical effort of a gate (namely, the ratios between the input capacitances), the ULE method is intuitive when analyzing the expressions for determining the optimal size of each gate, as shown below in .

The optimum condition represented by (13) addresses resistive interconnect, which usually refers to long and intermediate wires. In the case of short local wires, the interconnect effort may be simply analyzed by only considering the capacitive component. The same analysis can be applied to the branches of logic gates. The optimal condition of electrical effort for minimal delay (13) reduces to the case of capacitive interconnect as described by the following expression

$$g_i \cdot h_i = g_{i+1} \cdot (h_{i+1} + h_{w_{i+1}}). \quad (14)$$

For a logic path without wires ($h_{w_i} = 0, R_{w_i} = 0$), the optimum conditions of ULE, (13) and (14), converge to the optimum of LE [1]: $g_i \cdot h_i = g_{i+1} \cdot h_{i+1}$. Note that the primary difference between LE and ULE optima for capacitive wires is the presence of the capacitive interconnect effort $h_{w_{i+1}}$. As the right part of the condition expresses the effort applied to gate $i+1$ by the load, the left part represents the relative driving ability. Thus, the factor $h_{w_{i+1}}$ is added as the contribution of the wire to the load of gate $i+1$.

Optimal Gate Size Derivation in ULE

The driving ability of a gate is related to the size of the gate and can be represented by a ratio of input capacitances. The optimum condition in (13) can be rewritten in order to derive the expression for the optimal input capacitance of each gate using the ULE model,

$$\left(g_{i-1} + \frac{R_{w_{i-1}} \cdot C_{i-1}}{R_0 \cdot C_0} \right) \cdot \frac{C_i}{C_{i-1}} = g_i \cdot \left(\frac{C_{i+1}}{C_i} + \frac{C_{w_i}}{C_i} \right), \quad (15)$$

$$C_i = \sqrt{\frac{g_i}{g_{i-1} + \frac{R_{w_{i-1}} \cdot C_{i-1}}{R_0 \cdot C_0}} \cdot C_{i-1} \cdot (C_{i+1} + C_{w_i})} = \underbrace{\sqrt{C_{i-1} \cdot C_{i+1}}}_{\text{LE}} \cdot \underbrace{\sqrt{1 + \frac{C_{w_i}}{C_{i+1}}}}_{\text{wire capacitance}} \cdot \underbrace{\sqrt{\frac{g_i}{g_{i-1} + \frac{R_{w_{i-1}} \cdot C_{i-1}}{R_0 \cdot C_0}}}}_{\text{logical efforts and wire resistance}}. \quad (16)$$

Note that the first part of the resulting expression is similar to the condition described by the LE model for a path of identical gates. The second component expresses the influence of the interconnect capacitance. The last component is related to the resistance of the wire and the difference between the individual logical efforts (types of logic gates) along the path.

In the case of a capacitive wire or branch, the expression of optimal gate capacitance reduces to

$$C_i = \sqrt{C_{i-1} \cdot C_{i+1}} \cdot \sqrt{1 + \frac{C_{w_i}}{C_{i+1}}} \cdot \sqrt{\frac{g_i}{g_{i-1}}}. \quad (17)$$

Calculation of Optimal Gate Sizes

The expression for the optimal capacitance in (13) illustrates the quadratic relation between the size of neighboring gates. The optimal gate size based on ULE can be determined by solving a set of N polynomial expressions for N gates along the path.

In order to reduce the complexity of the solution, a relaxation method can be used. The technique is based on an iterative calculation along the path while applying the optimum conditions:

- a. (Initialization) Set the gate capacitances along the path to arbitrary values (only the first and last values are given).
- b. (Iteration) Replace each capacitance by the value derived by applying the optimum expression (13) on the two neighboring logic gates.
- c. (Stop check) If any of the new values differ by more than a given precision from the previous value, reiterate step b.

An example of optimal gate sizing is listed in Table 1 for a logic path composed of eight NAND gates with 0.1 mm wires and output load of $10C_0$. When observing the accuracy after each iteration, note that 5% accuracy is reached after three iterations. Also note that the gates in the last few stages of the path are the first to converge, since the accuracy increases while propagating along the path. Consequently, fewer calculations are performed in each successive iteration.

iteration	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
0	1	1	2	3	4	5	6	7	10
1	1	5.8	12.9	17.2	18.9	19.4	19.6	22.0	10
2	1	6.8	16.6	23.0	25.2	25.9	26.6	23.8	10
3	1	7.1	17.8	24.8	27.2	28.0	27.5	24.0	10
4	1	7.1	18.1	25.3	27.8	28.3	27.6	24.0	10
5	1	7.2	18.2	25.5	27.9	28.4	27.6	24.0	10

Table 1. Gate sizes calculation by relaxation. Wire segment length $L_i = 0.1$ mm. The values are normalized to $C_0 = 0.73$ fF.

Additional Derivations from ULE Model

The optimum condition (13) can be used to determine the optimal *equal scaling* factor x_{opt} , defined as the ratio of the gate size to a minimum-size inverter. This factor is used in optimization heuristics involving segmentation of the wires by general logic gates [14], where all of the gates are of equal sizes ($h_i = 1$) and equal wire segments. An additional application of x_{opt} is the case of long logic paths, where the differences in size are negligible ($\lim_{i \rightarrow \infty} h_i \rightarrow 1$).

Equation (13) can be rewritten for the electrical effort $h_i = 1$ and equal logical effort g of the gates along the logic path:

$$\left(g + \frac{R_{w_i} \cdot C_i}{R_0 \cdot C_0} \right) \cdot 1 = g \cdot \left(1 + \frac{C_{w_i}}{C_i} \right). \quad (18)$$

The resulting optimum for sizing of a general gate is

$$x_{opt} = \frac{C_i}{C_0} = \sqrt{\frac{R_0 \cdot C_{w_i}}{R_{w_i} \cdot C_0}} \cdot g \quad (19)$$

Note that x_{opt} is independent of the wire length for a given technology since the factor C_{w_i}/R_{w_i} is independent of wire length. For the special case of repeater insertion (inverters with an electrical effort $g = 1$), the condition in reduces to

$$x_{opt} = \sqrt{\frac{R_0 \cdot C_{w_i}}{R_{w_i} \cdot C_0}} \quad (20)$$

This optimal scaling factor is similar to optimal repeater scaling described by Bakoglu in [3].

V. EXAMPLES

The ULE technique has been applied to several example logic paths to demonstrate the properties of optimal gate sizing. The optimizations have been performed using parameters from [18] for a 65 nm CMOS technology with the following values:

<i>Minimal inverter</i>	$R_0 = 8800 \, \Omega$, $C_0 = 0.74 \, \text{fF}$
<i>Intermediate wires</i>	$r_w = 1.0 \, \Omega/\mu\text{m}$, $c_w = 0.15 \, \text{fF}/\mu\text{m}$
<i>Global wires</i>	$r_w = 0.04 \, \Omega/\mu\text{m}$, $c_w = 0.23 \, \text{fF}/\mu\text{m}$

The examples start from the special case where all of the gates have the same logic function and all of the wires have the same length L to demonstrate how ULE is related to existing optimization techniques. These examples are followed by more general examples of logic paths with different logic gates and wire segments. The circuits analyzed in the examples are presented in Fig. 4.

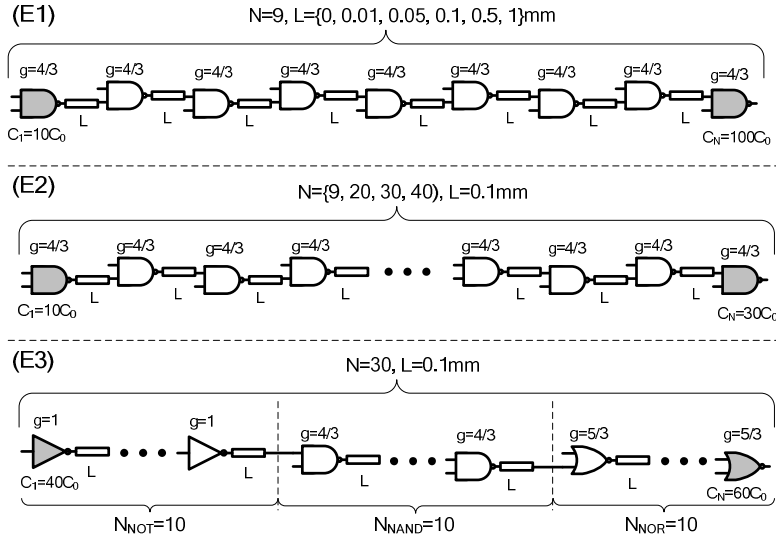


Fig. 4. Circuits used for ULE optimization examples.

The example logic path E1 consists of nine identical stages with wires of intermediate length. The input capacitance of the first and last gates are $10 \cdot C_0$ and $100 \cdot C_0$, respectively. The optimal size of the logic gates along the path are presented in Fig. 5 for several values of wire length L . ULE optimization provides an optimal solution for any range of wire length, and the special cases of long and short interconnects converge to existing techniques. All of the solutions range between two limits (the bold lines in the plot): (a) for zero wire lengths, the solution converges to LE optimization [1], and (b) for long wires, the gate size in the middle stages of the path converges to equal sizing, $x_{opt} = 49.6$ (the dashed line) as described in (19) resembling the repeater insertion methods [3][14]. While the LE solution (without wires) exhibits uniform gate size tapering, the long wire solution exhibits different tapering at the first and last stages, depending upon the input and load capacitances.

Note that the convergence to an optimum solution of equal sizing is not necessarily reached in all situations. This property depends upon the number of gates along the path. Equal sizing, however, is an asymptotic solution.

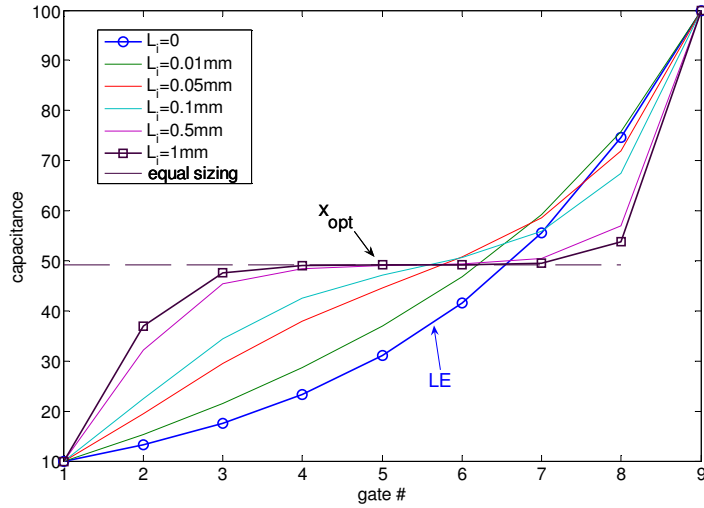


Fig. 5. Optimal ULE sizing (normalized with respect to C_0) in circuit E1 for several wire lengths at each stage. For zero wire length, the solution converges to LE optimization. For long wires, the solution converges to equal sizing x_{opt} .

The optimal solution of example circuit E2 is shown in Fig. 6 for a varying number of gates along the path. The input and output gate capacitances are $10 \cdot C_0$ and $30 \cdot C_0$, respectively. Each gate drives a wire segment of length $L = 0.1$ mm. When the logic path contains only nine gates, convergence to x_{opt} is not achieved. For paths with a larger number of gates, however, the convergence to equal sizing is reached for the middle stages along the path.

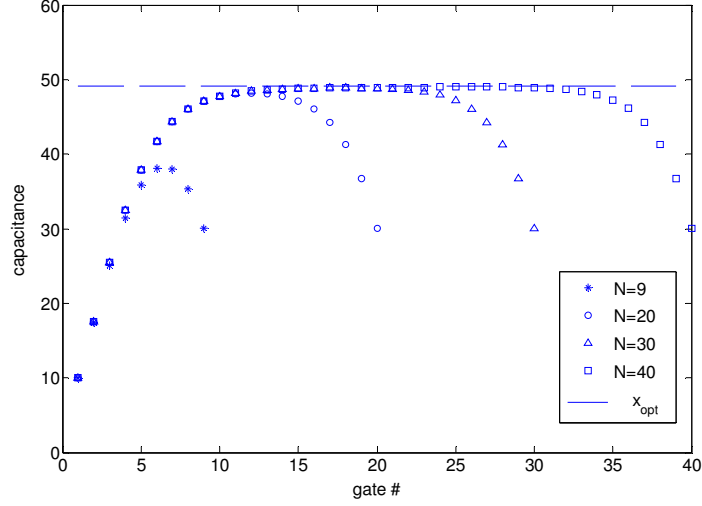


Fig. 6. Optimal ULE sizing (normalized to C_0) for circuit E2 with varying number of gates along the path. The convergence to optimal equal sizing depends upon the number of gates along the path. The optimum serves as an asymptotic solution.

The rate of convergence to equal optimal sizing depends upon the type of logic gate. The optimal size is determined by the logical effort of the gate and the parameters of the wire according to (19). The optimization results of circuit E3, are shown in Fig. 7 where the circuit is a 30-stage path consisting of three types of gates: ten inverters, ten NORs, and ten NANDs with equal intermediate wires. The input and output gate capacitances in this case are $40 \cdot C_0$ and $60 \cdot C_0$, respectively. Note that each type of gate converges to a different optimal size: $x_{opt_{NOT}} = 43$, $x_{opt_{NAND}} = 49.6$, $x_{opt_{NOR}} = 55.5$. Also note that the optimum solution of equal sizing does not depend upon the length of the wire segments. The wire length only influences the rate of convergence to equal sizing of the stages.

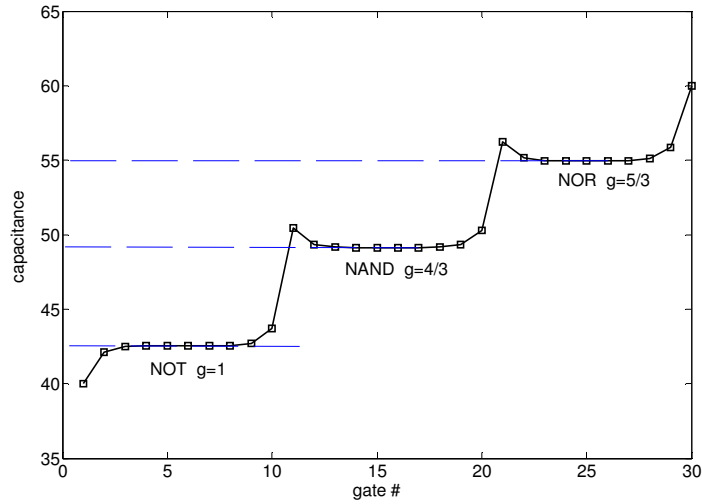


Fig. 7. Optimal ULE sizing (normalized with respect to C_0) vs. types of gates along a long path. Each type of gate converges to a different optimal equal size. The wire length only influences the rate of convergence but not the optimal size.

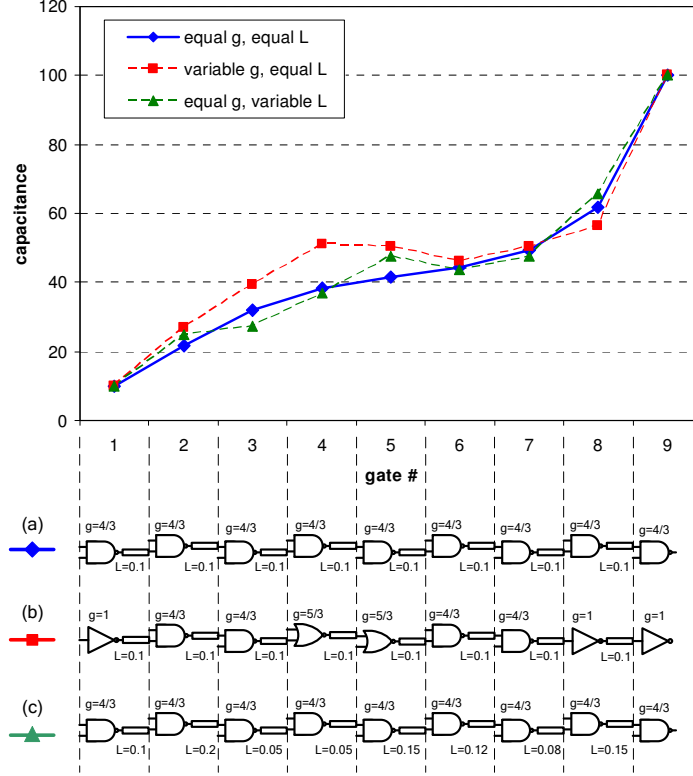


Fig. 8. Optimal ULE sizing (normalized with respect to C_0) (a) similar gates and equal wire lengths, (b) various gates and equal wire lengths, and (c) similar gates and various wire lengths. Those gates with higher logical effort have a higher scaling factor. Circuits with various gates and wires do not converge to x_{opt} .

In Fig. 8, the optimal sizing is shown for three circuits: (a) all of the gates along the path are of similar type (NAND) with equal logical effort ($g = 4/3$) and equal wire length, (b) the path contains various gates but equal wire length between each logic stage, and (c) the path contains similar gates but different wire length between each logic stage (the total wire length is equal in all cases). The optimal sizing changes as a function of g_i and L_i according to the optimization condition described by (16). Fluctuations in the input size can be observed in those cases where the neighboring gates along the path differ in logical effort. As a result of the difference in driving capability, those gates with higher logical effort have a relatively larger scaling factor. The difference in the wire length of the stages have a similar effect on the optimal gate size - a larger size is required for all of the gates to drive longer interconnect segments. Note that due to the difference in gate types and wire lengths, there is no convergence to a single equal size of logic gates.

VI. OPTIMAL NUMBER OF STAGES

As presented in the previous section, the proposed ULE model optimizes the timing of a logic path with a given number of stages by sizing the gates. Further delay minimization can be achieved by optimizing the number of stages, namely by inserting additional gates or buffers. The idea is similar to adding inverters to a logic path to obtain an optimal number of stages in LE, or to repeater insertion [3][14]. While in repeater insertion methodologies the buffers or gates can be placed anywhere along the wire; in many practical circuits the wire segments are fixed along the path after placement and routing (see Fig. 9a).

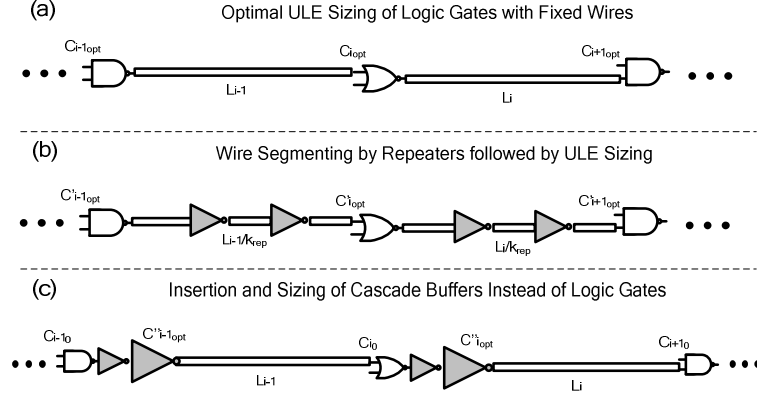


Fig. 9. Techniques for determining the optimal number of stages: (a) ULE sizing is performed on gates with fixed wires, (b) repeaters can be inserted along wires, and (c) cascade buffers can be added and sized to maintain small size logic gates.

The first optimization heuristic that can be incorporated into ULE is based on repeater insertion within long wire segments along a path (see Fig. 9b). In this case, wires are divided into shorter segments by repeaters prior to ULE sizing. The number of repeaters is determined from [3]. After repeater insertion, ULE optimization is performed to determine the optimal size of the individual logic and repeater gates.

Another optimization step can be performed in addition to repeater insertion. The optimal size of logic gates that drive long interconnect can be large, expending excessive area and power. This effect is most significant in multiple input logic gates where all of the transistors have to be scaled in order to obtain the optimum condition if one of the inputs is along the critical path. This problem can be solved by using buffers to drive the long wire segments, as shown in Fig. 9c. In order to minimize delay, the buffers should have a cascade structure with tapered inverters. The optimal number of inverters in each cascade can be determined from the LE model [1] since the wires impedance between the cascaded inverters is negligible. Sizing of the entire path can be determined from ULE.

VII. SUMMARY

Delay optimization in logic paths with wires has become an important issue in VLSI circuit design. The interconnect is now the dominant factor in performance-driven circuits and must be considered explicitly during the optimization process. The characteristics of the wires are not correlated with the characteristics of the gates; not allowing the use of the standard logical effort model. In fact, optimal gate sizing in the presence of interconnect does not correspond to equal effort of all of the stages along the path.

The Unified Logical Effort (ULE) method is proposed here for delay evaluation and minimization of logic paths with general gates and RC wires. The ULE method provides closed-form conditions for minimum delay. The ULE method converges to the LE conditions in cases of zero interconnect, and yields optimal equal sized gates when long wires are considered, as in repeater insertion methodologies.

Optimal gate sizing is provided by the ULE method, making ULE suitable for both manual calculations as well as for integration into CAD tools. The technique is applied to several example logic paths, permitting the influence of the wire length, gate type, and technology parameters to be evaluated.

The ULE method can be combined with known heuristics for buffering and repeater insertion. This combination is practical due to the fixed wire lengths that are dictated in many design flows. Further research is required to determine closed-form solutions that combine simultaneous optimal gate sizing with wire segmentation.

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