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Power-Optimal Ordering of Signals in Parallel Wire Bundles

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***Abstract* — A computationally efficient technique for reducing interconnect active power is presented. Power reduction is accomplished by simultaneous wire spacing and net ordering, such that cross-capacitances are optimally shared. The existence of a unique power-optimal wire order within a bundle is proven, and a closed form of this order is derived. The optimal order of wires depends only on the activity factors of the underlying signals; hence it can be performed prior to spacing optimization, without affecting the optimality of the combined solution. The proposed algorithm has been applied to various interconnect layouts, including wire bundles from high-end microprocessor circuits in 65nm technology. Interconnect power reduction up to 37% has been observed in such bundles.**

***Index Terms*— routing, wire ordering, wire spacing, power optimization, interconnect optimization**

I. INTRODUCTION

With the advancement of semiconductor technology, power dissipation becomes an important design objective. Interconnect power, which is the power dissipated by charging and discharging of wire capacitances, typically represents about 50% of the circuit's dynamic power [2]. Therefore, the optimization of interconnect power is an important VLSI design challenge. Interconnect power can be expressed by

$$P_{tot} \propto \sum_{i=1}^{N} C_i \cdot V_{DD} \cdot V_i \cdot f \cdot AF_i \,, \qquad (1.1)$$

where summation is done over all N nodes of the circuit, C_i is the interconnect capacitance at node i, V_i is the voltage swing at node i, f is the clock frequency and AF_i is the activity factor of node i. Common power reduction techniques are based on architectural, logic or circuit design methods, decreasing f, AF_i, N or V_i [3], [4], [6]. Bus coding techniques for reducing activity and wire cross-capacitance has also been used [5], [7], [8], [10].

In this paper we propose a technique for reduction of interconnect power by reducing the capacitance term C_i in(1.1) for the most active nodes within parallel wire bundles. Wire bundles are common in modern VLSI circuits global interconnect structures. The capacitances in such structures (see Fig. 1) are typically dominated by cross-capacitances between adjacent wires, since the aspect ratio of wire thickness to wire spacing grows with the progression of manufacturing technology [25].

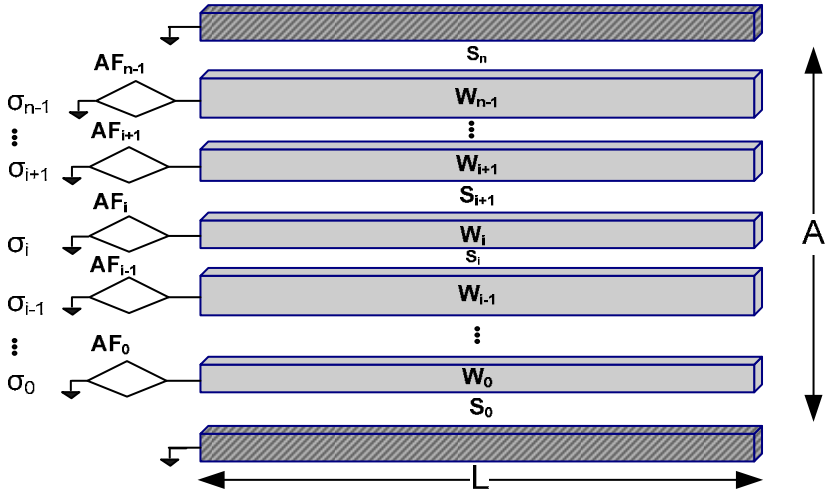

Fig. 1 Model of interconnect bundle of parallel wires. The $i-$th wire has activity AF_i, width W_i spaces to the neighbors S_i and S_{i+1}. The total bundle length is L and routing area is A

The proposed method sets the physical positions of the signals in the bundle in order to obtain optimal sharing of inter-wire capacitances. Unlike encoding which works in the logic domain, adding special logic which consumes area and increases delay, the method proposed in this paper works in the physical layout domain and doesn't consume any extra area or sacrifice any delay.

Optimal cross-capacitance sharing is achieved by space allocation and wire reordering according to signals' activity factors. Signals with high activity should be loaded by small cross-capacitances, which implies large spaces. Low-activity signals can tolerate smaller spaces. In order to best utilize the given area, which is a constrained resource, high-activity signals should be placed near each other and share the large spaces, while low-activity signals will share small spaces.

The method is illustrated in Fig. 2. There, a bundle contains some signals with high activity (H) and some others with low activity (L). The ordering in Fig. 2(b) is superior to Fig. 2(a), which is apparently the worst. Wire spacing optimization aiming at minimizing the total power will yield smaller (better) power for configuration 2(b), as compared to 2(a).

Signal ordering is effective when signal activities are known a priori, as in the case of an address bus. In common design practice signals are laid out sequentially from the least significant bit, which is the most active, to the most significant bit, which is typically the least active when sequential addresses are used. However, the ordering which minimizes power consumption is the one where least significant bits are positioned at the center of the bundle and the two most significant bits are positioned on the two sides of the bus, as illustrated in Fig. 3. When some signals in a bundle require shielding, it is beneficial to place them near the sidewalls of the bundle and order the rest of the signals in the central area, according to their activity factors.

Although net-ordering and spacing for delay and cross-talk noise reduction has been discussed widely in the literature [9], [11], [12], [14], [16], [17], [19], it has been addressed very superficially for power optimization. Coupling capacitance has been addressed explicitly in the context of physical design for minimizing dynamic power in [1], [13], [20], [21], [22]. Swapping of wires for power reduction was applied in [1], [20], [22]. In [22], the authors used a similar approach to the one described in this paper,

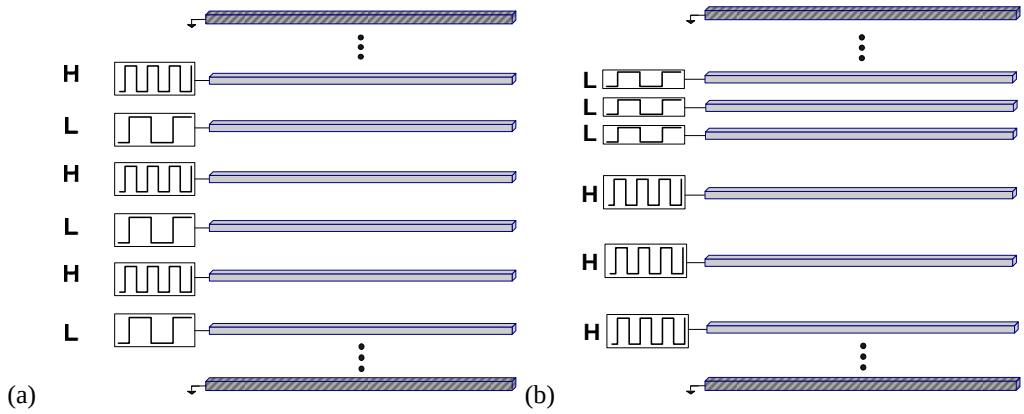

Fig. 2 Space sharing in two interconnect bundle configurations. a) Interleaved placement of wires with high (H) and low (L) activity, b) Wires are grouped according to signal activities.

based on intuition and heuristics. This paper presents a mathematically proven solution, yielding simultaneously the optimal ordering and optimal space allocation for the signals of a wire bundle.

II. OPTIMAL NET ORDERING AND SPACING FOR POWER MINIMIZATION

Consider a bundle of n signal nets $\sigma_0,...,\sigma_{n-1}$ residing between two side-walls (wires at fixed locations, connected to V_{cc} or V_{dd}) as shown in Fig. 1. W_i, S_i and S_{i+1}, respectively, denote width and spaces to neighbors of wire σ_i. The length of each wire is L. The distance A between the side walls is predefined and needs to satisfy the following constraint:

$$g\left(\bar{W},\bar{S}\right)=\sum_{j=0}^{n-1}W_i+\sum_{j=0}^{n}S_i=A. \tag{2.1}$$

Assuming full voltage swing at each node, the power consumed by wire i is:

$$P_i=AF_i\left(\alpha LW_i+\delta L\left(\frac{MCF_i}{S_i}+\frac{MCF_{i+1}}{S_{i+1}}\right)+\gamma L\right)V_{dd}{}^2 f\,, \tag{2.2}$$

where α,δ,γ are coefficients of area, coupling and fringe capacitances, V_{dd} is supply voltage and f is the clock frequency. AF_i is the activity factor of σ_i and MCF_i is the Miller Coupling Factor between the $i-1$-th and i-th wire. Rearrangement of (2.2) yields:

$$P_i=AF_i\left(aW_i+b\left(\frac{MCF_i}{S_i}+\frac{MCF_{i+1}}{S_{i+1}}\right)+P^0\right), \tag{2.3}$$

where $a=\alpha LV_{dd}{}^2 f$, $b=\delta LV_{dd}{}^2 f$, and $P^0=\gamma LV_{dd}{}^2 f$.

The mathematical technique used below to minimize the power is based on a timing-optimization approach described in [18]. The treatment of MCF for power is different than for timing. For timing the design must satisfy minimum and maximum delay requirements, hence minimum and maximum values of MCF are used for critical paths. What counts for power is the average MCF. According to Miller's theorem the simultaneous switching of two signals in identical and opposite directions yields MCF of 0 or 2, respectively (Fig. 4). Therefore an average MCF of 1 is assumed for internal bundle wires. For the side nets

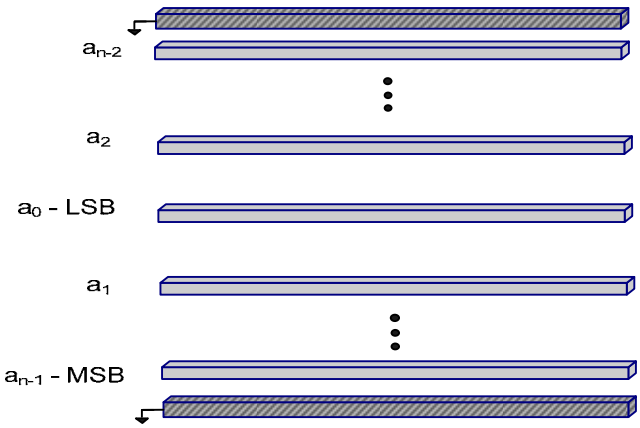

Fig. 3 Optimal ordering of address bus. The LSB, which has largest activity, is placed in the middle. The MSB, with lowest activity, is placed near wall.

σ_0 and σ_{n-1}, the MCF is also 1, since the sidewall wires are shields.

Substituting MCF=1 in (2.3) and summing over all signals yields the following total interconnect active power:

$$P\left(\overline{W},\overline{S}\right)=\sum_{i=0}^{n-1}P_i=a\sum_{i=0}^{n-1}AF_i\cdot W_i+b\sum_{i=1}^{n-1}\frac{AF_{i-1}+AF_i}{S_i}+\frac{AF_0\cdot b}{S_0}+\frac{AF_{n-1}\cdot b}{S_n}+nP^0 \tag{2.4}$$

Assume for the moment that the order π of the signals in the bundle is given. To minimize (2.4) subject to (2.1) differentiate P and g by all of their sizing variables. Let's assume that wire widths are allocated in advance according to other design considerations, such as design rules, wire delays or electro-migration effects, and therefore they are not part of the optimization. Notice that from a pure power viewpoint, disregarding timing, minimum power is achieved by setting $W_i=W_{\min}, 0\le i\le n-1$. Thus we differentiate P and g only by variables S_i, which results in the following spacing at minimizing total power for a given order π [18]:

$$\begin{cases} S_i=\sqrt{\dfrac{b}{\lambda}\left(AF_{i-1}+AF_i\right)}, & 0<i<n; \\ S_0=\sqrt{\dfrac{b}{\lambda}AF_0}; & \\ S_n=\sqrt{\dfrac{b}{\lambda}AF_{n-1}} & \end{cases} \tag{2.5}$$

where λ is a positive constant (Lagrange multiplier).

Let Π denote the set of all wire permutations in the bundle and consider now $\pi\in\Pi$ as variable. Let π^* denote the permutation for which the optimal wire spacing yields minimum total power among all $\pi\in\Pi$. One needs therefore to solve the problem:

Minimize: $P(\pi,\overline{W},\overline{S})$, subject to: $\sum_{j=0}^{n-1}W_i+\sum_{j=0}^{n}S_i=A$.

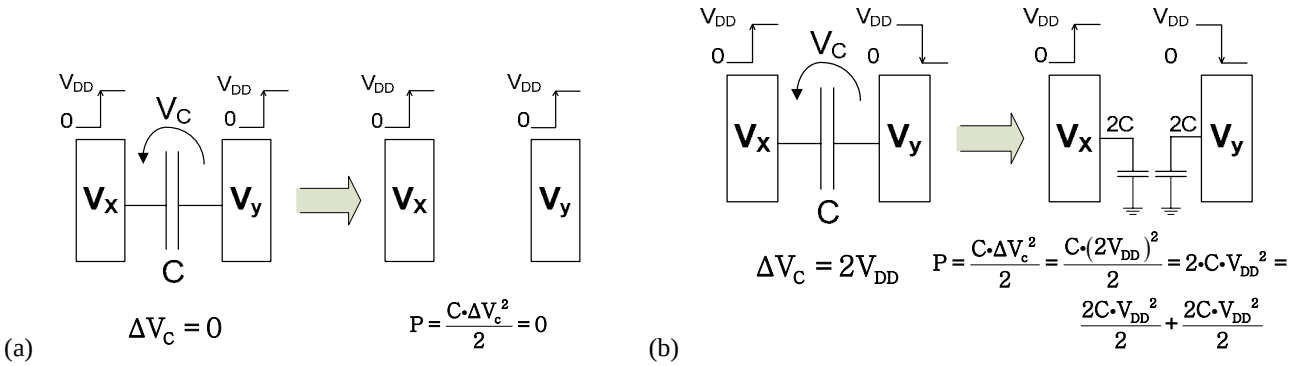

Fig. 4 Miller's theorem for power. (a) Miller's theorem for simultaneous switching of two wires in the same direction – MCF = 0; (b) Miller's theorem for simultaneous switching of two wires in opposite directions – MCF = 2.

In this formulation, both signal ordering and wire spacing are optimized simultaneously.

Substitution of (2.5) into (2.4) produces the following expression for the minimal power at a given permutation:

$$P = a\sum_{i=0}^{n-1} AF_i \cdot W_i + \frac{b}{A - \sum_{i=0}^{n-1} W_i}\left(\sum_{i=1}^{n-1}\sqrt{AF_{i-1} + AF_i} + \sqrt{AF_0} + \sqrt{AF_{n-1}}\right)^2 + nP^0 = P^I + P^{II}$$

where

$$P^I = a\sum_{i=0}^{n-1} W_i \cdot AF_i + nP^0$$

and

$$P^{II} = \frac{b}{A - \sum_{i=0}^{n-1} W_i}\left(\sum_{i=1}^{n-1}\sqrt{AF_{i-1} + AF_i} + \sqrt{AF_0} + \sqrt{AF_{n-1}}\right)^2. \qquad (2.6)$$

The term P^I is invariant for any ordering of the signals. In term P^{II} the indices of adjacent signals interact with each other in square root terms, thus making P^{II} dependent on the order of signals in the bundle. The reason for this interaction is the cross capacitance between adjacent wires, caused by the space they share with each other.

The mathematical properties of the expressions of the kind (2.6) were discussed thoroughly in [18] in context of minimizing the total sum of weighted delays. Fortunately, equation (2.6) which describes the order-dependent portion of the total bundle power, is similar to the order-dependent portion of total weighted delay discussed in [18].

Consequently, the order of wires which minimizes the total bundle power is obtained as follows. Signal nets are sorted in ascending order of activity factors $AF_0 \le AF_1 \le \cdots \le AF_{n-2} \le AF_{n-1}$. The sorted set is split into even and odd subsequences $AF_0 \le AF_2 \cdots$ and $AF_1 \le AF_3 \le \cdots$. By reversing the order of numbers in the odd subsequence it becomes a monotonic decreasing sequence. Finally, the even and the modified (reversed) odd subsequences are concatenated into one sequence. The new sequence thus obtained is said

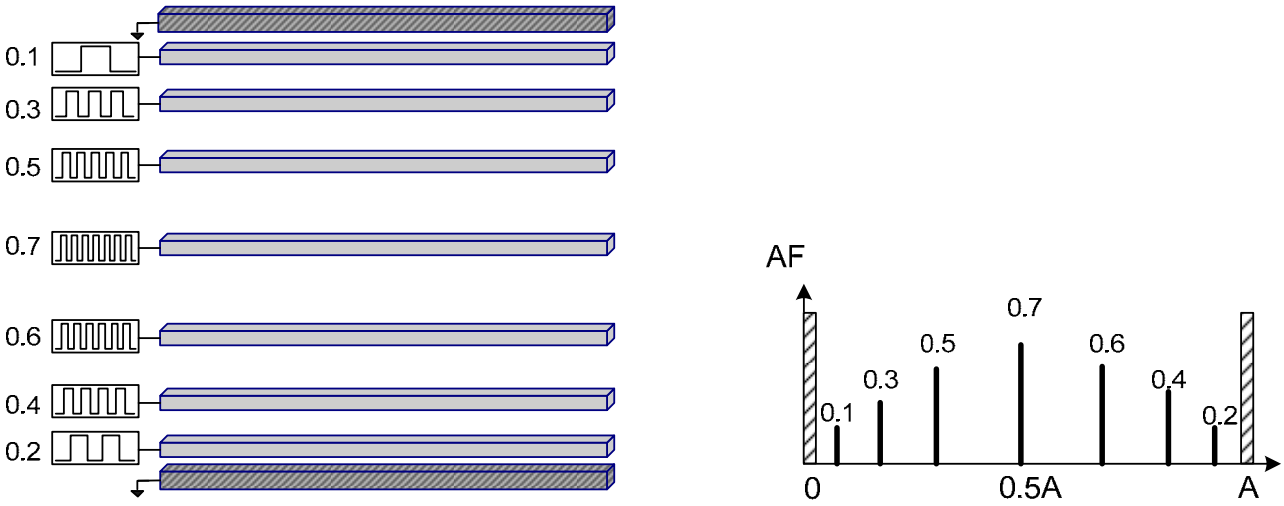

Fig. 5 Symmetric hill ordering by Activity Factors. On the left: an interconnect bundle with wires placed in symmetric hill order and spaced for minimum power: the most active wire is in the middle with maximal spacing and the least active wires are near the walls with minimal spacing. On the right: net activity vs. wire location within the bundle.

to be ordered in ***symmetric hill ordering*** *by activity factor* (as it resembles climbing and descending a symmetric hill). Fig. 5 illustrates such an order.

III. EXPERIMENTAL RESULTS

Two experiments have been performed for 65nm process technology.

Experiment 1: *Impact of area allocated to the wire bundle on power reduction by reordering*. The routing pitch of a given layer $X = W_{\min} + S_{\min}$ is defined as the sum of min width and min space (usually they are equal). When the area allocated to an n-signal bundle is $A = nW_{\min} + (n+1)S_{\min}$, wire reordering will not reduce power since the wire to wire spacing is always minimal, regardless of their order in the bundle. On the other hand, allocating excessive bundle width that allows very large spacing between any two adjacent wires is also almost insensitive to wire ordering. Setting bundle width between these extreme cases enables significant power reduction, as demonstrated in the following experiment.

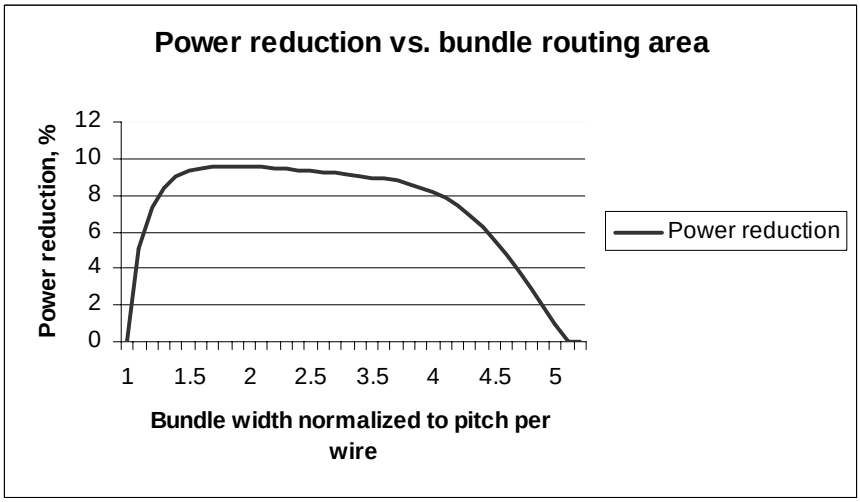

Fig. 6 Power reduction vs. bundle width . For width less than a single pitch per wire or larger than 4.7 pitches per wire (on average) the power reduction is zero in this example, since all spaces must be identical in these ranges because of maximum or minimum spacing constraints.

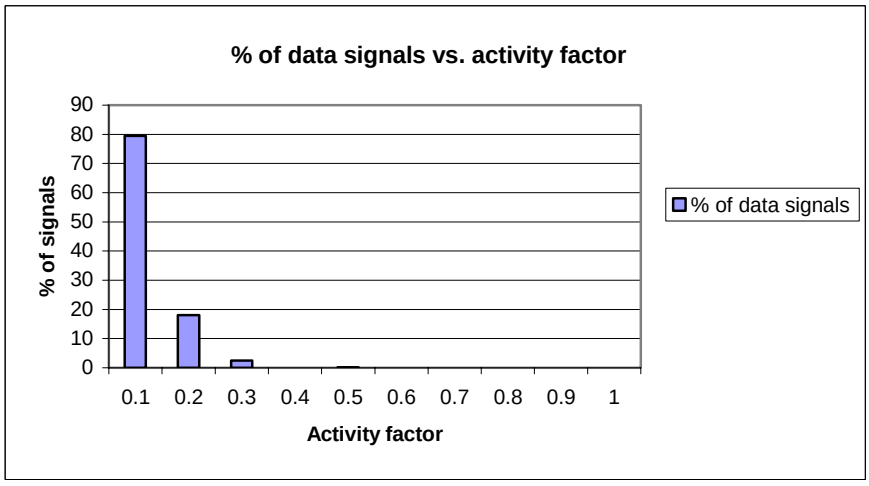

Fig. 7 Distribution of data signals by activity factor. More than 95% of the signals have activity less than 0.2

The experiment was conducted in 65nm process technology with the following parameters: bundle length $L = 300\mu m$, 4th metal layer, for which $W_{\min} = S_{\min} = 0.14\mu m$ and $n = 5$. The 5-signal bundle width was set from $\frac{2n+1}{2n} = 1.1$ pitch / wire up to 5 pitches / wire, which is an excessively large area allocation. For every value of bundle area 100 random sets of 5 activity factors were drawn and the average power reduction was calculated. The results are shown in Fig. 6. There, the maximum reduction is 10%, achieved at allocation of 2 pitch / wire. Indeed, this is a very common setting of VLSI interconnect buses, having wire width and space of twice the minimum.

Experiment 2: *Power optimization by net reordering and spacing in an industrial design.* This experiment

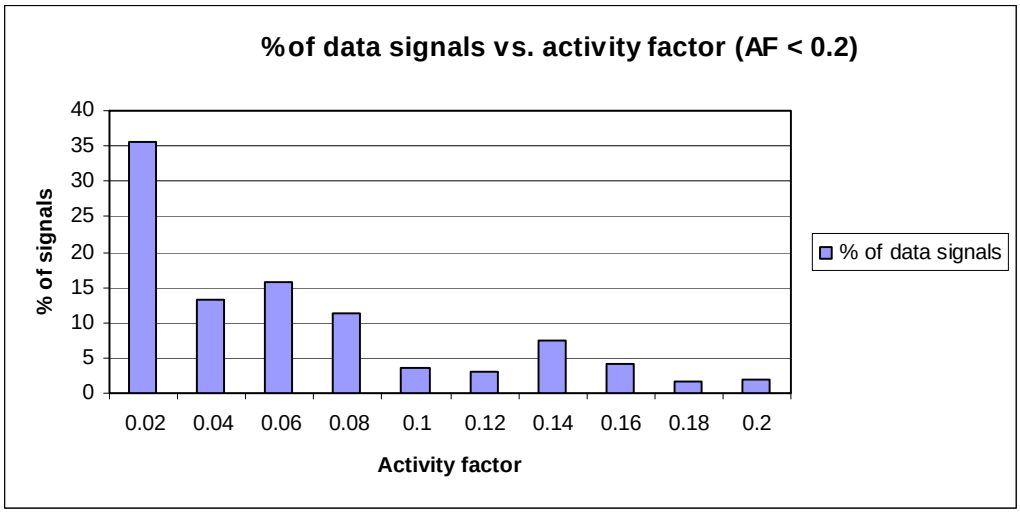

Fig. 8 Distribution of data signals by activity factor for signals with activity less than 0.2.

was conducted on a circuit block from a high-end microprocessor designed in 65nm process technology. Activity factors of signals were derived using industrial tools that run a suite of benchmark test cases on a representative block of the design. Fig. 7 shows that 80% of the signals have activity of less than 0.1, while the activity of more than 95% of the signals is less than 0.2. Further expansion of the distribution for the low activity signals is shown in Fig.8.

A typical layout snapshot is shown in Fig.9, exhibiting typical interconnect signal bundles extending across the underlying block. Some bundles are shown at a larger zoom. Dark colored signals have low activity while light ones are of higher activity. The specific parameters of each magnified bundle are shown in table I.

For each of these bundles ordering and spacing optimization have been performed. First, spacing optimization has been performed and the power reduction was recorded. Then the bundles were reordered according to the underlying activity factors and spacing optimization was re-invoked, and the power reduction was recorded again. As expected, the second space optimization yielded larger reduction than the first. This improvement in power reduction is attributed to wire ordering. Results are presented in Fig. 10. The total optimization impact varies from 9% to 37% with 17% on average. The average gain attributed to spacing only is 12%, while average gain attributed to ordering is 5%.

TABLE I. PARAMETERS OF BUNDLES DERIVED FROM THE LAYOUT

Number of bundle (number of signals in brackets)	1 (6)	2 (6)	3 (4)	4 (5)	5 (5)
Metal layer	3	3	4	2	2
Bundle length, μm	150	184	173	96	98
Bundle width, μm	1.77	2.105	2.94	1.7	1.7
Signal activity factors	0.064; 0.014; 0.023; 0.097; 0.005; 0.014	0.066; 0.063; 0.062; 0.065; 0.178; 0.204	0.025; 0.045; 0.004; 0.023	0.059; 0.205; 0.073; 0.159; 0.066	0.158; 0.06; 0.066; 0.075; 0.204

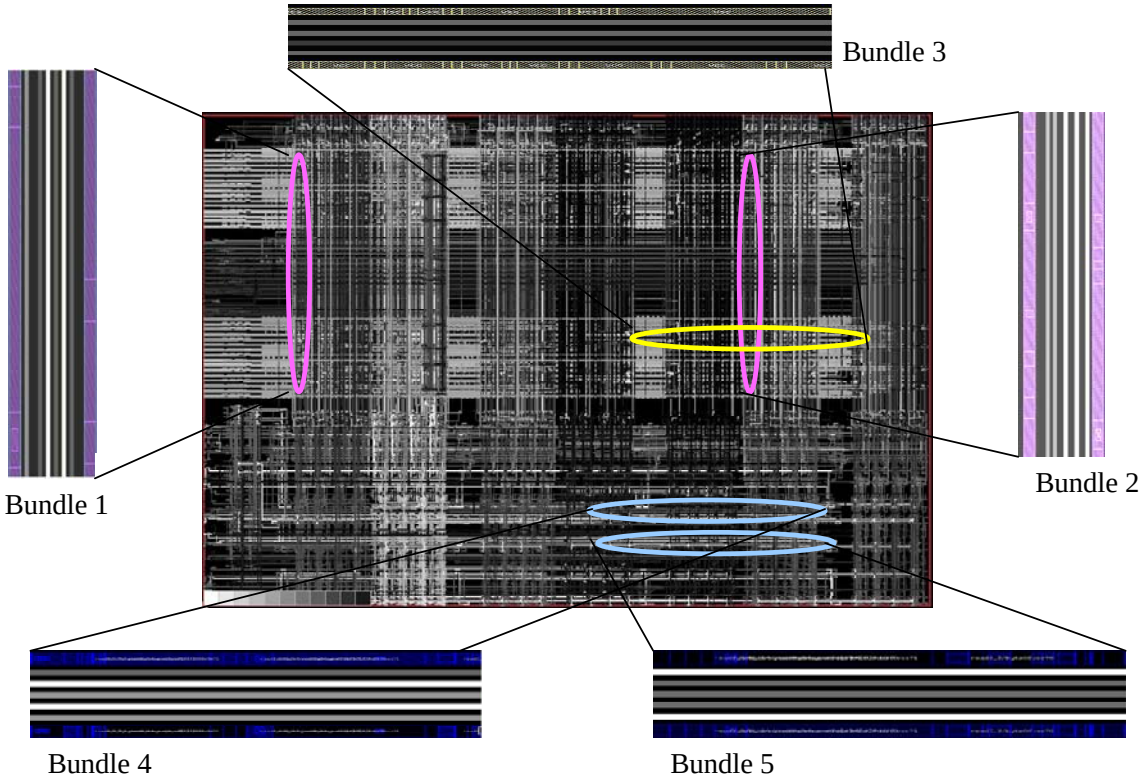

Fig. 9 Snapshot of a processor data path block. Signals are colored according to their activity factors from 0 (black) to 0.2 (white). Bundles chosen for optimization are shown on the picture.

IV. DEPENDENCE OF OPTIMIZATION IMPACT ON TECHNOLOGY PROCESS

As lateral feature sizes decrease with technology advancement, an important question is how bundle power will be affected by net ordering in future manufacturing process technology generations. Let's analyze the ratio P^{II}/P^{I}. The larger this ratio is, the more effective wire ordering is. Substituting expressions for a, b and P^0 in (2.3) into(2.6) yields:

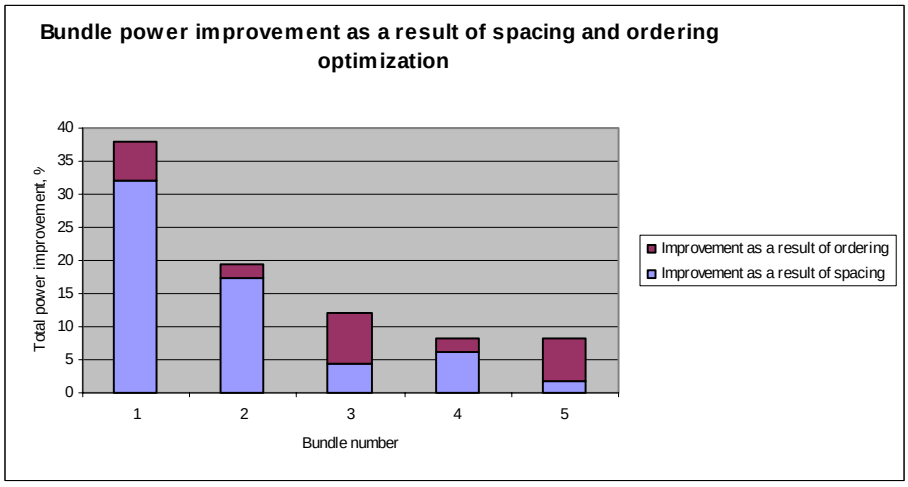

Fig. 10 Power reduction as a result of spacing and ordering optimizations

$$\frac{P^{II}}{P^{I}} = \frac{\left(\sum_{i=1}^{n-1}\sqrt{AF_{i-1}+AF_i}+\sqrt{AF_0}+\sqrt{AF_{n-1}}\right)^2}{A-\sum_{i=0}^{n-1}W_i}\cdot\frac{\delta L}{\alpha L\cdot\sum_{i=0}^{n-1}AF_iW_i+\gamma nL}. \tag{4.1}$$

The term $k=\left(\sum_{i=1}^{n-1}\sqrt{AF_{i-1}+AF_i}+\sqrt{AF_0}+\sqrt{AF_{n-1}}\right)^2$ is independent of layout and technology, hence

$$\frac{P^{II}}{P^{I}} = \frac{k}{A-\sum_{i=0}^{n-1}W_i}\cdot\frac{\delta}{\alpha\cdot\sum_{i=0}^{n-1}AF_iW_i+\gamma n} \tag{4.2}$$

Denote by $\overline{AF}=\frac{1}{n}\sum_{i=0}^{n-1}AF_i$ the average activity factor, and assume for convenience that all wires have the same width W. Substitution into(4.2) yields

$$\frac{P^{II}}{P^{I}} = \frac{k}{n\left(A-nW\right)}\cdot\frac{\delta}{\alpha W\overline{AF}+\gamma} \tag{4.3}$$

Wire ordering becomes more effective as the ratio (4.3) becomes larger. Let's check dependence of (4.3) on technology parameters.

For a first-order analysis, the ratios $\frac{\alpha}{\delta}$ and $\frac{\gamma}{\delta}$ are approximated by $\frac{1}{t_{ox}H}$ and $\frac{1.06}{\sqrt{t_{ox}H}}$ [24] .Thus, the ratio can be expressed as:

$$\frac{P^{II}}{P^{I}} = \frac{k}{n(A-nW)}\cdot\left(\frac{1}{t_{ox}H}W\cdot\overline{AF}+\frac{1.06}{\sqrt{t_{ox}H}}\right)^{-1} = \frac{k}{n\left(\frac{A}{W}-n\right)}\cdot\left(\frac{1}{AR_m\cdot AR_v}\cdot\overline{AF}+1.06n\cdot\frac{1}{\sqrt{AR_m\cdot AR_v}}\right)^{-1} \tag{4.4}$$

where $AR_m = \frac{H}{W}$ and $AR_v = \frac{t_{ox}}{W}$ are aspect ratios (thickness of material / minimum width) of a metal line and a via, respectively.

Table II has been derived from ITRS reports [25], predicting these values for several technology generations ahead. Both are increasing from generation to generation. The parameters of equation (4.4) such as A, W, n and $\overline{AF}$ were derived from design data shown in Table I. Substitution into (4.4) shows that the ratio P^{II}/P^{I} steadily increases, thus making the ordering optimization more effective with process technology evolution (last row of Table II).

TABLE II. INCREASE OF METAL AND VIA ASPECT RATIOS IN FUTURE TECHNOLOGIES

Year of production	2005	2007	2009	2011	2013	2017
Metal 1 ½ pitch, nm	90	68	52	40	32	20
Metal AR (AR_m)	1.7	1.8	1.8	1.8	1.9	2
Via AR (AR_v)	1.5	1.6	1.6	1.6	1.7	1.8
P^{II} / P^{I}	0.111	0.118	0.118	0.118	0.126	0.133

CONCLUSION

The total switching power of interconnect wire bundles in a single metal layer within a limited width is typically dominated by cross-capacitances between adjacent wires, and can be improved by simultaneous net spacing and ordering according to signal activity factors. The optimal order of signals within the bundle depends only on their activity factors, taking the form of a symmetric hill Order. Numerical experiments have shown that the effectiveness of wire reordering strongly depends on the width allocated to the interconnect wire bundle. The largest reduction was achieved at the allocation of about two pitches per average wire. The power saving obtained by the spacing and ordering combined optimization performed as post-processing on industrial layouts in 65nm process technology ranged from 9% to 37%. Although in terms of the entire power consumption this turns into a smaller percentage, it is still significant. It is highly recommended to apply wire ordering optimization at the early stages of design and apply it as a guideline for the routing tool in use.

REFERENCES

[1] E. Macii, M. Poncino and S. Salerno, "Combining Wire Swapping and Spacing for Low-Power Deep-Submicron Buses", Proc.of the 13th ACM Great Lakes symposium on VLSI, pp. 198-202, 2003

[2] N. Magen, A. Kolodny, U. Weiser and N. Shamir, "Interconnect-power dissipation in a microprocessor", *in Proc. of the 2004 international workshop on System level interconnect prediction*, pp. 7-13, Paris, 2004

[3] H. Zang, V. George, and J.M. Rabaey, "Low-swing on-chip signaling techniques: effectiveness and robustness", *IEEE Trans. on VLSI Systems*, Vol.8, No. 3, pp. 264-272, June 2000

[4] C. Hsieh and M. Pedram, "Architectural Power Optimization by Bus Splitting", *Proc. of DATE 2000*, pp. 612-616, Paris, 2000

[5] D. Bertozzi, L. Benini, and G. De Micheli, "Low power error resilient encoding for on-chip data buses", *Proc. of DATE 2002*, p. 102, 2002
[6] L. Shang, L. Peh, and N. Jha, "Power-efficient Interconnect Networks: Dynamic Voltage Scaling with Links", *Computer Architecture Lectures*, Vol. 1, Issue 1, 2002
[7] L. Benini, G. De Micheli, E. Macii, D. Sciuto, and C. Silvano, "Address Bus Encoding Techniques for System-Level Power Optimization", *DATE 1998*, pp. 861-866, Paris, 1998
[8] K. Kim, K. Baek, N. Shanbhak, C. Liu, and S. Kang, "Coupling-Driven Signal Encoding Scheme for Low-Power Interface Design", *Proc. of ICCAD 2000*, pp. 318-321, 2000
[9] A. Kahng, S. Muddu, E. Sarto and R. Sharma, "Interconnect Tuning Strategies for High-Performance ICs", *Proc. Design, Automation and Testing in Europe*, Paris, February 1998.
[10] M. Cha, C. Lyuh, and K. Kim, "Low Power Bus Encoding With Crosstalk Delay Elimination", *IEE Proc.-Comput. Digit. Tech*., Vol. 153, No. 2, March 2006
[11] S. S. Sapatnekar, "Wire Sizing as a Convex Optimization Problem: Exploring the Area Delay Tradeoff*"*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 8, pp. 1001 - 1011, August 1996.
[12] J. Cong, L. He, C. K. Koh and Z. Pan, "Interconnect Sizing and Spacing with Consideration of Coupling Capacitance", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 9, pp.1164-1169, September 2001.
[13] R. Arunachalam, E. Acar, and S. R. Nassif, “Optimal shielding/spacing metrics for low power design”, Proceedings of IEEE Computer Society Annual Symposium on VLSI, pp. 167-172, 2003.
[14] P. Gupta and A. Kahng. "Wire Swizzling to Reduce Delay Uncertainty Due to Capacitive Coupling." *Proc. IEEE Intl. Conf. on VLSI Design*, January, p.431, 2004
[15] S. Wimer, S. Michaely, K. Moiseev and A. Kolodny, "Optimal Bus Sizing in Migration of Processor Design", *IEEE Transactions on Circuits and Systems – I*, vol. 53. no. 5, May 2006.
[16] M. L. Mui, K. Benerjee and A. Mehortra, "A global interconnect optimization scheme for nanometer scale VLSI with implications for latency, bandwidth, and power dissipation", *IEEE Transactions on Electron Devices*, Vol. 51, No. 2, Feb. 2004, pp. 195-203.
[17] K. Moiseev, S. Wimer, A. Kolodny, "Timing optimization of interconnect by simultaneous net-ordering, wire sizing and spacing", *Proc. of IEEE international symposium on Circuits and Systems*, pp. 329-332, June 2006
[18] K. Moiseev, S. Wimer, A. Kolodny, " On Optimal Ordering of Signals in Parallel Wire Bundles", INTEGRATION – the VLSI journal, in press, 2007.
[19] K. Jhang, S. Ha, and C. John, "A segment rearrangement approach to channel routing under the crosstalk constraints", *Asia-Pacific Conf. on Circuits and Systems*, pp. 536-541, 1994
[20] C. Lyuh, T. Kim , and K.Kim, "Coupling-aware high-level interconnect synthesis for low power", *Proc. of ICCAD 2002*, pp. 609-613, 2002
[21] M. Ghoneima, Y. Ismail, "Delayed line bus scheme: a low-power bus scheme for coupled on-chip buses", *Proc. of 2004 international symposium on Low power electronics and design*, pp. 66-69. 2004
[22] Y. Shin and T. Sakurai, "Coupling-Driven Bus Design for Low-Power Application-Specific Systems", *Proceedings of the 38th conference on Design automation*, pp. 750-753, 2001
[23] F. Najm, "Improved Estimation of the Switching Activity for Reliability Prediction in VLSI Circuits", *Custom Integrated Circuits Conference*, pp. 429-432, 1994
[24] E. Barke, "Line-to-ground Capacitance Calculation for VLSI - A Comparison", *IEEE Transactions on CAD*, vol. 7, no. 2, pp. 295-298, 1988.
[25] 2005 ITRS report, available online http://www.itrs.net/reports.html