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Digital Implementation of An SPC Decoder for Gigabit Rates

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Abstract

A robust implementation of a soft-decoding single parity check code (SPC) decoder for error correcting in high speed communication is proposed in this work.

A concatenated coding approach which has been proposed [1] and studied in many recent works [2], [5] provides coding gain comparable with those achieved with Viterbi decoding but with a simpler implementation. The most popular scheme recommended for high rate, low complexity is concatenating soft decision decoded single parity check inner code (9,8) with a (255, 223, 16) Reed-Solomon outer code. A coding gain of 4.8 dB is achieved at a bit error rate of 10^{-5} with an overall code rate of 0.78 [2].

To date Reed-Solomon and Viterbi decoders work up to 40 Mb/sec. It is possible to implement a single high data rate SPC soft decoder with several multiplexed Reed Solomon or Viterbi outer decoders.

The design of the SPC decoder presented here was successfully implemented in the Technion Communication Lab with commercial TTL technology, and proved to be robust up to 30 Mb/sec. Technology is available now for implementing this scheme for data rates up to 10 Gb/sec with commercial GaAs components.