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A Low Power Video Processor

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Abstract

Recent advances in VLSI technology led to increased introduction and use of portable electronics devices. These devices call for low power circuits in order to prolong their battery life span. One example is the video processor for CCD camcorders. In this paper we investigate various power reduction techniques as applied to such a video processor. In particular, we limit the study to methods that are useful for the ASIC designer, who cannot affect the process, device and circuit levels but is limited to designing with a given library of standard cells.

We have found that some RTL and architectural level methods, including asynchronous design, dynamic voltage scaling, bus switching minimization, pipeline stage merging, reduction of switching times and clock gating, failed to save power. This is attributed to the relative small size and low clock frequency of the video processor; those methods would typically be more effective for larger and faster chips.

Instead, we have successfully applied an application-specific, algorithmic level method. High inter-pixel correlation, characteristic of video images, allowed us to operate on pixel differences, which are typically zero or small numbers. This approach yielded 3-15saving, depending on image types.

A base-line design and a pixel-difference processor were both implemented in RTL, synthesized with Synopses using a 0.35 micron CMOS library, and analyzed using PowerMill. Simulations were performed with multiple sample images, and verified with a functional simulator written in C++. We believe that the results are accurate to within 5