CCIT Report No. 303

1/f Noise in CMOS Transistors for Analog Applications

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ABSTRACT

Noise measurements of the 1/f noise in p-mos and n-mos transistors for analog applications are reported under wide bias conditions ranging from subthreshold to saturation. Two "low noise" CMOS processes of $2\mu m$ and $0.5\mu m$ technologies are compared and it is found that the more advanced process, with $0.5\mu m$ technology, exhibits significantly reduced 1/f noise, due to optimized processing. The input referred noise and the PSD of the drain current 1/f noise are modeled in saturation as well as in subthreshold and are compared with the common empirical approaches such as the SPICE models. The results of this study are useful to the design and modeling of 1/f noise of CMOS analog circuits.