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Two Priority Buffered Multistage Interconnection Networks

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***Abstract*— This paper presents a novel architecture of internally two priority buffered Multistage Interconnection Network (MIN). First, we compare by simulation the new architecture against a single priority MIN and demonstrate up to N times higher high-priority throughput in a hot spot situation, when N is the number of inputs. In addition, under uniform traffic assumption we show an increase in the low priority throughput, without any change in the high priority throughput. Moreover, while in the single priority system the high priority delay and its standard deviation are increased when low priority traffic is present, it is kept constant in the dual priority system. Finally, we introduce a new approach of long Markovian memory performance model to better capture the packets dependency in a single priority MIN under uniform traffic and extend this model for a dual priority MIN. Model results are shown to be very accurate.**

I. INTRODUCTION

In recent years, there has been much interest devoted to incorporating multimedia applications in packet switching networks. Different types of traffic need different QoS standards, but share the same network resources, such as buffers and bandwidth. For real-time applications, it is important that mean delay and delay-jitter are bounded, while for non real-time applications, such as data transfer, the loss ratio often is the restrictive quantity.

A priority service scheme can be defined in terms of a policy determining: (a) which of the arriving packets are admitted to the buffer(s); and/or (b) which of the admitted packets is served next. The former priority service schemes are typically referred to as space priority (or discarding) schemes and attempt to minimize the packet loss of loss-sensitive traffic, such as data. An overview and classification of some space priority strategies can be found in [1, 2]. The latter priority service schemes are typically referred to as time priority (or priority scheduling) schemes and attempt to guarantee acceptable delay boundaries to delay-sensitive traffic, such as voice and video. Several types of time priority schemes, such as Weighted-Round-Robin and Weighted-Fair-Queueing, have been proposed and analyzed, each with their own specific algorithmic and computational complexity, see for example [1] and [3] and the references therein.

There are already several commercial switches which accommodate traffic priority schemes, see for example [4, 5]. These switches consist of an internally single priority switch fabric and employ two priority queues for each input port. Packets are queued based on their priority level and packets with higher priority number are allowed to pass first. Chen and Guerin [6] studied an N×N internally one priority non-blocking packet switch with input queues. They assumed that high priority packets preempt low priority ones at the input and move ahead of all low priority packets waiting for service at their input queue. They also assumed that high priority packets always prevail over low priority packets contending for the same output. Given these assumptions and the fact that the switch is non-blocking, they suggested that the presence of low priority packets is transparent to high priority ones, for which the switch behaves as a single priority switch, and studied the performance of low priority packets. They determined the total maximum throughput and established that it can exceed that of an equivalent single priority switch. Ng and Dewar [7] introduced a simple modification to a load sharing replicated banyan networks to guarantee priority traffic transmission. They considered two switch planes, such that one switch plane is designated as the high priority traffic switch plane, and the other is designated as the low priority traffic switch plane. Their simulation results show that when the high priority traffic constitutes less than 30% of the total traffic, one can guarantee extremely low packet loss for the high priority traffic. In addition, when the high priority to low priority traffic ratio increases, the distinction between high and low priority traffic performance decreases. In general, they observed that the high priority traffic delay and packet loss were significantly lower than those of the low priority traffic.

The internal switch structure used in all the above studies is a single priority fabric with controlled inputs. In contrast to these previous works, our paper considers for the first time an internal two priority switch fabric architecture and focuses on the effect of a two priority input buffered Multistage Interconnection Network (MIN) on the performance of high and low priority traffic. We also suggest a new Markovian model for analyzing the performance of the two priority traffic types, assuming uniform traffic, and present numerical results.

A MIN consists of a number of stages of small switching elements (SE), which are interconnected by a permutation function. An (N×N) delta-a network [8] consists of n stages of

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