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ACCMP - Asymmetric Cluster Chip Multi-Processing

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Abstract— Achieving high performance within a power envelope becomes extremely difficult as feature sizes decrease. Uniprocessor architects encounter diminishing returns when trying to attain higher performance in exchange for area and power. For multithreaded programs, symmetric chip multiprocessing (CMP) offers higher throughput and power efficiency than uniprocessors. However, symmetric CMP does not scale well with technology. In this paper we explore the theoretical advantages of placing asymmetric core clusters in multiprocessor chips. All of the cores on the ACCMP die have the same instruction set architecture, but may have a completely different micro-architecture. We show that asymmetric core clusters are expected to achieve higher performance per area and higher performance for a given power envelope.

***Index Terms*— ACCMP, Multiprocessing.**

I. Introduction

Power consumption is becoming extremely important as microprocessors become more complex. The constant decrease in feature sizes enables processor architects to improve processor performance by using the extra silicon real estate. Due to wire delays and increased architectural complexity, uniprocessor performance does not scale well with the increase of the effective processor die area. Additionally, uniprocessors are becoming extremely power inefficient, as 1% of performance increase costs approximately 3% in additional power consumption. Since the power consumption envelope and the power density of current microprocessors are approaching or have even reached in some cases their limits, a new design paradigm must be employed.

Symmetric chip multiprocessing (CMP) aims to increase performance while increasing the power and area proportionally. CMP processors divide the threads of multithreaded applications among the symmetric cores, exploiting their parallelism. Although single-threaded applications may run slower on a CMP, modern desktop and server operating systems run multiple threads, making the overall performance higher. Most leading microprocessor manufacturers are either already offering CMP processors or have announced plans to do so [1].

When adding an additional core to a symmetric CMP chip, 1% of power and 1% of area are exchanged for roughly 1% of performance, given that we ignore thread contention. This can be seen in Figure 1. However, it is possible to pay less than 1% of power for each one percent of performance, by placing asymmetric [2] core clusters on one die. General purpose threads will be executed on the larger core clusters, while the smaller core clusters will be highly tuned for specific application domains, such as streaming applications (media, data encryption...), virus checking, data mining, etc. Due to their smaller size and their tuned architecture, addition of smaller cores can provide a performance advantage of better than 3% for each 1% in power. This can be seen in Figure 2.