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Optimal Bus Sizing in Migration of Processor Design

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Abstract

The effect of wire delay on circuit timing typically increases when an existing layout is migrated to a new generation of process technology, because wire resistance and cross capacitances do not scale well. Hence, careful sizing and spacing of wires is an important task in migration of a processor to next generation technology. In this paper, timing optimization of signal buses is performed by resizing and spacing individual bus wires, while the area of the whole bus structure is regarded as a fixed constraint. Four different objective functions are defined and their usefulness is discussed in the context of the layout migration process. The paper presents solutions for the respective optimization problems and analyzes their properties. In an optimally-tuned bus layout, after optimizing the most critical signal delay, all signal delays (or slacks) are equal. The optimal solution of the MinMax problem is always bounded by the solution of the corresponding sum-of-delays problem. An iterative algorithm to find the optimally-tuned bus layout is presented. Examples of solutions are shown, and design implications are derived and discussed.