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Net-Ordering for Optimal Sharing of Cross-Capacitances in Nanometer Interconnect Design

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ABSTRACT

This paper addresses the problem of ordering and sizing parallel wires in a single metal layer within an interconnect bus of a given width, such that cross-capacitances are optimally shared for circuit delay minimization. Using an Elmore delay model including cross capacitances for a bundle of fixed-width wires, we show that an optimal wire ordering is uniquely determined, such that best timing can be obtained by proper allocation of inter-wire spaces. The optimal ordering, called BMI (Balanced Monotonic Interleaved) depends on the size of drivers, and is independent of size of receivers. The paper also addresses the problem of simultaneously ordering and optimizing variable-width wires. A heuristic approach for wire ordering and sizing is presented. Examples for 90-nanometer technology are analyzed and discussed.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Design Styles – *Microprocessors;* B.7.2 [**Integrated Circuits**]: Design Aids – *Placement and Routing.*

General Terms

Performance, Design.

Keywords

routing, wire ordering, wire spacing.

1. INTRODUCTION

Cross-capacitances between wires in interconnect structures have a major effect on circuit timing. The importance of this effect grows with technology scaling. Since cross-capacitance between two wires depends on inter-wire spacing and affects the delays of both wires, allocation of inter-wire spaces and wire widths becomes an optimization problem for bus structures under a total area constraint [1]. This paper addresses a more general problem, where delays in a bundle of parallel wires (with different drivers and loads) are minimized by choosing an optimal

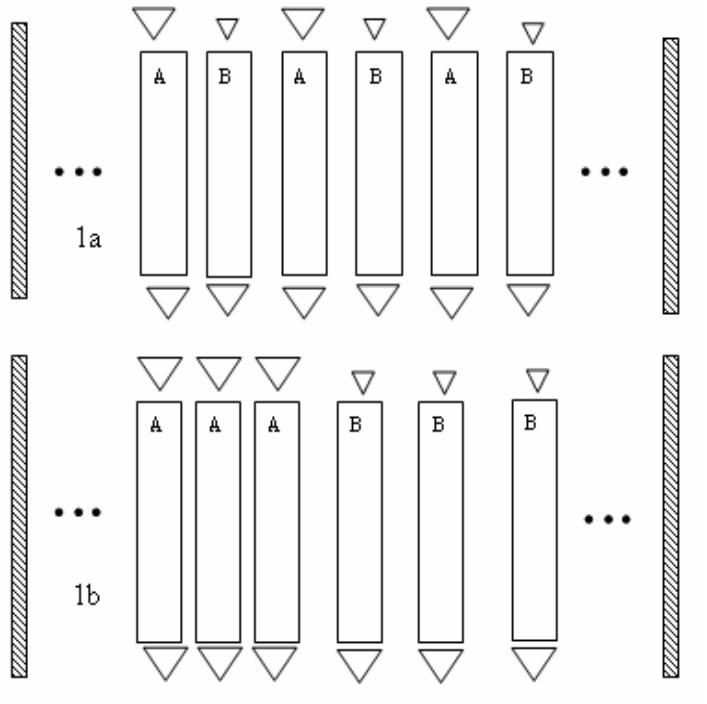

Figure 1. a. – interleaved placement of wires; b – sorted placement of wires