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Fast Asynchronous Bit-Serial Interconnects for Network-on-Chip

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***Abstract*—The multiple wires required for on-chip bit-parallel interconnect in large systems on chip (SoC) occupy large chip area and present a significant capacitive load. The problem is exacerbated in Networks-on-Chip (NoC), which employ numerous multi-bit links with widely varying throughput demands, activity rates and standby periods. We approach this challenge with high speed on-chip serial interconnects. Conventional differential-signaling serial link circuits, typically employed for chip-to-chip I/O communications, are inappropriate for on-chip serial links, since they require complex clock and data recovery PLL-based circuits, which consume excessive power and area. Instead, we investigate low power asynchronous data transfer techniques, based on low voltage differential transition signaling. A novel bit-serial interconnect structure, comprising encoder, serializer, de-serializer and decoder circuits, is described and analyzed. Low latency synchronizers are employed at each end, enabling seamless connectivity of separate clock domains. Asynchronous NoC routers can be inserted along the link in a modular fashion, rendering this design useful for scalable NoC architectures. Dynamic and leakage power, as well as area, compare favorably with other link architectures.**

Index Terms—NoC, Serial Interconnect, Asynchronous Circuits, Differential Signaling, Low-Swing, Dual-Rail, Two-Phase, 1-of-2 Encoding, NRZ encoding**.**

I. Introduction

Large Systems on Chip (SoC), comprising a large number of modules, typically require multiple long on-chip data channels that interconnect far-away modules. Bit parallel data links provide high data rates at the cost of large chip area, routing difficulty, and high dynamic power. In addition, such links are often utilized over only a small portion of the time, but dissipate leakage power at all times. Leakage is incurred at the line drivers and also at the repeaters, which are often necessary for long interconnects.

Bit-serial interconnects address the issues of chip area, routability, and leakage power, since there are fewer wires, fewer line drivers, and fewer repeaters. However, data rate is reduced due to serialization, and hence serial links can be employed