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Efficient Routing in Irregular Topology NoCs

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Abstract

Networks on a Chip (NoC) commonly employ an irregular mesh topology because of variations in module sizes and shapes. Consequently, low cost routing techniques such as XY routing are inadequate, raising the need for low cost alternatives. In this paper we first define a hardware resource based cost model for comparing different routing mechanisms. Next, we propose three hardware efficient routing methods for irregular mesh topology NoCs. Our methods combine a fixed routing function (such as XY or "don't turn") and reduced size routing tables based on the known distributed and source routing techniques. For each method, we develop path selection algorithms that minimize the overall cost. Finally, we demonstrate by simulations a significant cost saving compared to standard solutions and examine the scaling of cost savings with the growing NoC size.

1. Introduction

Modern VLSI systems on Chip (SoCs) comprise many system modules. According to technology projections [1,2] the number of modules will grow to several hundreds in the near future. NoCs were shown to be effective for solving the global interconnect problem among modules [3-10]. NoC power and area saving along with QoS considerations have led to the common use of mesh topology along with static, destination based shortest path (SP) routing, using minimal amount of router logic [4-7]. In a regular mesh it is easy to accomplish shortest path routing, by employing a simple variation of a deadlock free dimension order routing [11] such as X-Y [4-7]. XY is also a "table-less" routing discipline whereby each packet is routed first in an "X" direction and then along the perpendicular dimension.

Practical NoC topologies become irregular meshes (Figure 1) because of modules shape and size variability in VLSI layouts and the need to physically separate between the modules internals and the NoC infrastructure. Nevertheless, to the best of our knowledge no previous studies addressed the problem of efficient static routing in irregular mesh NoCs.

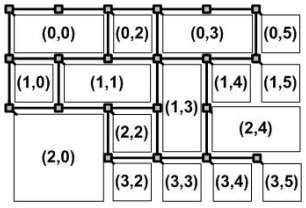

Figure 1. SOC modules interconnected by irregular mesh NoC

Our definition of an irregular mesh topology is that it is identical to the full mesh including the addresses used to identify the various modules, except that that some routers and links are missing (Figure 1). Packet routing in such NoCs resembles routing in a labyrinth, since some links are missing and may lead to a dead-end. Therefore, a simple X-Y scheme cannot be employed and different routing techniques need to be applied. In other networks, routing in irregular topologies is typically accomplished using routing tables (RT). The RTs can be located in routers (distributed routing) or in sources (source routing). RT size and the corresponding power and area costs grow with the network size. Moreover, the time required to access each table, which affects NoC performance, depends on its size and thus on the network size.

We introduce a simple metric for the estimation of VLSI cost (area and power) of NoC routing based on the total size of the routing tables. Then, we develop novel, hardware-efficient routing techniques that reduce the VLSI cost of routing in irregular–mesh topology NoCs. The techniques are based on a combination of a fixed routing function (such as "route XY" or "don't turn") and reduced routing tables for both distributed and source routing approaches. The entries in the reduced routing tables are created only for destinations whose routing decisions differ from the output of the routing function. This way, we significantly reduce the area and power costs of full routing tables in most cases. Our routing algorithms perform routing path extraction for all source-destination pairs, together with minimization of the VLSI cost of the packet routing logic. We do not treat the deadlock problem, since there are standard ways to solve it after all static routes are selected [11]. Random simulations of different topologies and communication scenarios are used for comparing and estimating the VLSI cost savings obtained by different algorithms. We also check the scaling of the VLSI cost savings in NoCs with growing numbers of modules and compare the scalability of distributed and source routing techniques in NoC with growing number of destinations.

2. Traditional Static Routing Techniques

Traditional static routing techniques can be classified according to where routing information is held and where routing decisions are made.

In *distributed routing* (DR) each packet carries the destination address, e.g. the X-Y coordinates of the destination router or a module number. The routing decision can be implemented in each router either by looking up the destination address in a routing table (memory) or by executing a routing function in hardware. Using this method, each network router contains a predefined routing table or routing function logic whose input is the destination address of the packet and its output is the routing decision. When the packet arrives at the input port of the router, its output port is looked up in the table or calculated by the routing logic according to the destination address carried by the packet. The routing information regarding each destination is captured in the