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Unified Logical Effort - A Method for Delay Evaluation and Minimization in Logic Paths with *RC* Interconnect

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***Abstract* - A model for delay evaluation and minimization in logic paths with gates and *RC* wires is presented. The method, *Unified Logical Effort* (ULE), provides closed-form conditions for timing optimization while overcoming the breakdown of standard logical effort (LE) rules in the presence of interconnect. The ULE delay model and optimization unifies the problems of gate sizing and repeater insertion: In cases of negligible interconnect, the ULE method converges to standard LE optimization yielding tapered gate sizes. In the case of long wires, the solution converges towards uniform optimal sizing of the gates as in repeater insertion methodologies. The technique is applied to various logic path examples , while investigating the influence of wire length, gate type, and technology. Techniques for combining the ULE method with existing heuristics of buffering and repeater insertion are also proposed.**

I. INTRODUCTION

Timing modeling and optimization is one of the main issues in high complexity circuit design. The method of logical effort (LE) was first proposed by Sutherland *et al.* [1] for fast evaluation and optimization of delay in logic paths (see Fig. 1a). The technique has since been adopted as a basis for many CAD tools, thanks to the simplicity of LE. The LE method benefits from an uncomplicated and intuitive delay model and closed-form optimization conditions. The optimization rule of logical effort, however, only addresses logic gates and does not consider on-chip wires. As VLSI circuits continue to scale, the contribution of wires to the delay increases and cannot be neglected. This characteristic occurs not only with respect to long wires interconnecting separate modules but also to inside of logic modules where the delays introduced by the wires interconnecting closely coupled gates approach and even exceed gate delays. The handy LE rule that the delay is minimum when the effort of each stage is equal breaks down, because interconnect has fixed capacitances which do not correlate with the characteristics of the gates (see Fig. 1b). This behavior is described by the authors of the LE method as "one of the most dissatisfying limitations of logical effort" [2].

The primary objective of this work is to develop a simple method for optimizing timing in logic paths containing both gates and interconnect. Currently, timing optimization is typically treated separately in two cases: (a) logic gates without wires (using the standard LE method), (b) long wires without logic (using