On Optimal Ordering of Signals in Parallel Wire Bundles

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Abstract — **Optimal ordering and sizing of wires in a constrained-width interconnect bundle are studied in this paper. It is shown that among all possible orderings of signal wires, a monotonic order of the signals according to their effective driver resistance yields the smallest weighted average delay. Minimizing weighted average delay is a good approximation for MinMax delay optimization. Three variants of monotonic ordering are proven to be optimal, depending on the MCF ratio between the signals at the sides of the bundle and that of the internal wires. The monotonic order property holds for a very broad range of VLSI circuit settings arising in common design practice. A simple, yet near-optimal, setting of wire widths within the bundle to yield the best average weighted delay is proposed. The theoretical results have been validated by numerical experiments on 65 nanometer process technology and industrial design data. In all cases the ordering optimization yielded improvement in the range of 10% in wire delay, translated to about 5% improvement in the clock cycle of a high-performance microprocessor implemented in that technology.**

Index Terms— **routing, wire ordering, wire spacing**

I. INTRODUCTION

Cross-capacitances between wires in interconnect structures have a major effect on circuit timing. The importance of this effect grows with technology scaling [1], [2]. In this paper, delays in a bundle of parallel wires with different drivers and loads are minimized by choosing an optimal ordering of the nets. A model for the bundle of wires is shown in Fig. 1(a). It represents a common CMOS layout configuration, where interconnect wires run in parallel between two power supply or shielding rails, such that the total width of the structure A is a fixed constraint. An abstraction of actual layout is made by assuming that all drivers and all receivers are located at the ends of the structure of length L. Real layouts can be decomposed into several such structures using effective drivers and receivers, since long segments of parallel wires are very common in industrial practice, mostly when high metal layers are concerned. The wire delays in the model of Fig. 1(a) are typically dominated by cross-capacitances between adjacent wires, since the ratio between wire thickness and wire width tends to grow with non uniform technology scaling [28]. Therefore, delays can be optimized by allocation of inter-wire spaces. In addition, wire widths can be set to optimize wire resistances. Furthermore, reordering of the wires can improve the timing, because critical wires can be put next to each other and share the largest spaces, which have the smallest cross-capacitances.

Reordering of the bundle wires is a new degree of freedom in timing optimization, which has not been explored in the past. The main result of this paper is that the signal ordering is highly beneficial and can