

Power-Optimal Ordering of Signals in Parallel Wire Bundles

Konstantin Moiseev², Shmuel Wimer^{1,2} and Avinoam Kolodny²

1. Intel Corporation, Israel Development Center, Haifa, Israel

2. Electrical Engineering Department, Technion, Haifa, Israel

Abstract — A computationally efficient technique for reducing interconnect active power is presented. Power reduction is accomplished by simultaneous wire spacing and net ordering, such that cross-capacitances are optimally shared. The existence of a unique power-optimal wire order within a bundle is proven, and a closed form of this order is derived. The optimal order of wires depends only on the activity factors of the underlying signals; hence it can be performed prior to spacing optimization, without affecting the optimality of the combined solution. The proposed algorithm has been applied to various interconnect layouts, including wire bundles from high-end microprocessor circuits in 65nm technology. Interconnect power reduction up to 37% has been observed in such bundles.

Index Terms— routing, wire ordering, wire spacing, power optimization, interconnect optimization

I. INTRODUCTION

With the advancement of semiconductor technology, power dissipation becomes an important design objective. Interconnect power, which is the power dissipated by charging and discharging of wire capacitances, typically represents about 50% of the circuit's dynamic power [2]. Therefore, the optimization of interconnect power is an important VLSI design challenge. Interconnect power can be expressed by

$$P_{tot} \propto \sum_{i=1}^N C_i \cdot V_{DD} \cdot V_i \cdot f \cdot AF_i, \quad (1.1)$$

where summation is done over all N nodes of the circuit, C_i is the interconnect capacitance at node i , V_i is the voltage swing at node i , f is the clock frequency and AF_i is the activity factor of node i . Common power reduction techniques are based on architectural, logic or circuit design methods, decreasing f , AF_i , N or V_i [3], [4], [6]. Bus coding techniques for reducing activity and wire cross-capacitance has also been used [5], [7], [8], [10].

In this paper we propose a technique for reduction of interconnect power by reducing the capacitance term C_i in (1.1) for the most active nodes within parallel wire bundles. Wire bundles are common in modern VLSI circuits global interconnect structures. The capacitances in such structures (see Fig. 1) are typically dominated by cross-capacitances between adjacent wires, since the aspect ratio of wire thickness to wire spacing grows with the progression of manufacturing technology [25].