CCIT Report #695 April 2008

Wire Spacing, Planar Graphs and the Minimization of Dynamic Power in VLSI Microprocessors

Konstantin Moiseev, Shmuel Wimer and Avinoam Kolodny

Abstract

The problem of optimal space allocation among interconnecting wires of VLSI chips, in order to minimize their switching power consumption is solved. Necessary and sufficient conditions for the existence of optimal space allocation are derived, stating that every wire must be in equilibrium of its line-to-line weighted capacitance density on its two opposite sides. Two proofs are presented, one based on convexity of the dynamic power objective, and another based on a graph representation of the problem. The notion of power density is introduced and it is proven that power is minimal if and only if its density is uniformly distributed across the entire layout. This condition is shown to be equivalent to all paths of the layout graph having the same length and all cuts having the same flow. An implementation which has been used in the design of a recent commercial high-end microprocessor is presented, and implications on circuit timing are discussed.

1. Introduction

The power consumed by VLSI systems is a significant factor in the design of new microprocessors and other products. The main reason for increased power dissipation is the growing logic complexity, with integration of multiple computational cores on a single die. The dissipation of power has become a major concern because of the growing awareness to environmental