

Assertion Based Verification of Multiple-Clock GALS Systems

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Abstract

Standard EDA ABV tools fall short of verifying multiple clock domain systems on chip (MCD SoC), asynchronous systems and Globally Asynchronous Locally Synchronous (GALS) systems. This paper describes a method for verifying asynchronous and multi-clock behavior in such systems using PSL and standard ABV tools. We convert STG (signal transition graphs), a common form for specifying asynchronous behavior, into PSL statements, employ standard ABV tools, and prove complete verification. The proposed ASE (automatic sequence extraction) algorithm was applied to a MCD SoC model that employed a network-on-chip (NoC) for asynchronous inter-modular communications.

1. Introduction

Large systems on chip (SoC) may incorporate multiple modules operating at different frequencies. Moreover, in dynamic voltage and frequency scaling (DVFS) systems, frequency and voltage may dynamically change during operation [1]-[3]. The resulting multiple clock domains (MCD) SoCs are treated as Globally Asynchronous Locally Synchronous (GALS) systems [4][5]. Inter-modular communications in MCD GALS systems are best implemented by asynchronous logic, eliminating multiple synchronization latencies and complex distribution of multiple clocks. Indeed, the ITRS predicts that by 2020 40% of SoC global signaling will be performed asynchronously [6]. However, to reliably employ asynchronous signaling, suitable verification techniques are required.

In a typical design and verification flow, the specification is converted into a design and also into verification statements (e.g. in PSL [7]). The design is typically verified with an ‘assertion based verification’ (ABV) tool [8]. ABV may be based on either simulation [9][12] or formal verification [13][14]. In addition, advanced ABV supports temporal expression and/or data validity verification (PSL, e-language, System-Verilog, etc.) [7]-[12]. However, this scheme is often limited to clocked designs that employ a single clock, due to language limitations and tool constraints. Thus, verification by ABV is usually inapplicable to MCD systems and to any asynchronous circuits that may be included in the design.

Verification techniques for pure asynchronous logic [15]-[20] mostly employ custom tools, complicating their integration into typical design and verification flows. GALS system verification and test method was discussed in [21], where a special test extension was added to each GALS wrapper. The test extensions disconnect locally synchronous islands during test data transfer between different GALS wrappers, allowing stand-alone massive testing of the wrappers and their interconnections. This technique appears to be more test-oriented. In [22] a GALS wrapper was modeled by Petri nets and verified for reachability and deadlock using model checking [23]. Clock domain crossing (CDC) verification was discussed in [24], where structural and functional synchronizer verification was performed using PSL. These references do not provide a complete verification method for GALS systems.