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Usage of Trace Cache for Predicting Power Saving Opportunities

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Abstract

The use of Trace Caches is a well known technique to overcome the problem of limited instruction fetch bandwidth in modern computer architectures. A Trace Cache stores instructions dynamically, based on the order of their execution, rather than the in the order they appear and are compiled within the source program. Trace Caches were found to be especially effective for very wide machines as they improve instruction fetch bandwidth.

Previous research projects propose the use of relatively short traces to increase the probability of the correct execution of the traces, as well as to optimize Trace Cache memory space utilization. In this research, we investigate the possibility of using the Trace Cache to achieve a reduction of power consumption within the design.

Power saving is an important aspect of modern architectures and many different algorithms have been proposed towards this goal. One of the proposed power saving techniques is dynamic tuning of processor's resources, by turning off, for example, those units and resources that are not in use. Implementing this technique requires a monitoring unit that is able to predict such down-time and provide information about the resources, as potentially needed by the execution. We propose to use a Trace Cache for that purpose, as traces, particularly lengthy ones, contain information about future instruction execution. Therefore, we believe we can use this information to optimize the execution of long and frequent-used traces, and suggest optimizations that can lead to major power savings.

To benefit from dynamic optimization, we need to be able to predict instruction sequences early enough in order to allow changes to the trace, allowing sufficient lead time to make the changes. Therefore, we focus on predicting long instruction sequences that will enable prediction of the processor needs for longer execution time. We will explore the feasibility of making dynamic optimizations based on the information about these sequences. We propose an algorithm for the dynamic tuning of processor's resources, based on the information stored within the Trace Cache. In our proposal, we aim to achieve this with minimal performance penalty and additional hardware requirements.

This work provides an overview of Trace Cache proposals and enhancements over existing solutions, including an overview of several power reduction techniques. We propose a novel opportunity for using long traces as a potential to reduce processor power consumption by analyzing the behavior of instructions that are executed from the Trace Cache. Finally, we discuss the possibilities of using the proposed algorithm.