

Dynamic Programming Algorithm for Interconnect Channel Sizing in Discrete Design Rules

Abstract

The lithography used for 32 nanometers and smaller VLSI process technologies restricts the admissible interconnect widths and spaces to very few discrete values with some interdependencies, making traditional interconnect sizing by continuous-variable optimization techniques impossible. Single-net bottom-up power-delay optimization for discrete wire widths has been solved and got a lot of attention in literature. This article presents a dynamic programming (DP) algorithm for interconnect width and space allocation yielding the optimal power-delay tradeoff function. It sets the width and spacing of all interconnects simultaneously, thus finding the global optimum. The DP algorithm is generic and can handle a variety of power-delay objectives, such as total power or delay, or weighted sum of both, power-delay product, max delay and alike. The algorithm consistently yields more than 10% dynamic power and 5% delay reduction for real data blocks designed in 32 nanometer process technology.

1. Introduction and Motivation

Power and delay of VLSI systems and their tradeoff is important design consideration of microprocessors and other products. The traditional pace of higher clock rate consumes more power, while recent demand for cool products is driving power reduction [1], [2]. Unfortunately power and delay conflict each other and their tradeoff is delicate and challenging, offering