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Timing aware power minimization in VLSI circuits by simultaneous multilayer wire spacing

K. Moiseev, A. Kolodny and S. Wimer

Abstract

Due to continuous technology scaling, the interconnect delay and power reduction is becoming one of the most important design challenges. In this paper, we present a novel algorithm for simultaneous multilayer interconnect spacing so that on the one hand the total power of interconnect is reduced and on the other hand, delay constraints are not violated. We first present an optimization problem and show that it is convex and therefore has unique optimal solution. Then, we develop algorithm which solves the optimization problem. The optimization we propose can be applied to individual nets as well as to large layouts due to smart layout partitioning scheme applied. We demonstrate algorithm effectiveness by showing power reduction of 5-12% of interconnect power on clips from real industrial layout of 32 nm technology node. In addition, we show relation of new optimization technique with previously reported Weighted Power-Delay Sum optimization (WPDS).

1. Introduction

The continuous scaling of technology process, trend towards mobile battery-operated electronic products and growing awareness to environmental heating have caused power minimization to become an important design challenge. Today, in order to produce power-efficient and high-speed VLSI products, power optimizations should be performed at all stages of the design flow: starting from architecture through RTL and circuit implementation and up to layout design. Generally, every opportunity to contribute to power saving is considered. On the other hand, circuit performance remains the most important design objective and power optimization cannot neglect timing constraints imposed on circuits. Therefore, any power optimization should be timing-aware, which is the topic of this paper.