CCIT Report #826 February 2013

Design Tradeoffs of Long Links in Hierarchical Tiled Networks-on-Chip

Ran Manevich[1] Leon Polishuk[1] Israel Cidon[2] Avinoam Kolodny[2]
Electrical Engineering Department, Technion – Israel Institute of Technology, Haifa, Israel.
{ranman, leonpol}@tx.technion.ac.il[1], {cidon, kolodny}@ee.technion.ac.il[2]

***Abstract* — Hierarchical topologies are frequently proposed for large Networks-on-Chip (NoCs). Hierarchical architectures utilize, at the upper levels, long links of the order of the die size. RC delays of long links might reach dozens of clock cycles in advanced technology nodes, if delay reduction techniques (e.g. wire sizing and repeater insertion) are not applied. Some proposals assume that long links can be adjusted to satisfy timing requirements but lack a deep evaluation of the tradeoffs and costs. Other proposals assume that long links must be pipelined, but do not provide a comprehensive justification.**

In this paper we evaluate the efficiency and the system costs of wire sizing and repeater insertion as methods to reduce link delays in hierarchical NoCs. We present a unified interconnect cost function that accounts for power and wiring overheads of these methods. Then, we quantify the costs of modifying long links in typical hierarchical NoCs for different target clock frequencies and technology nodes. Although long links might undergo aggressive adjustments, we find these overall costs to be low at the system level for many typical cases, taking into account that there are only a few long links in most proposed hierarchical NoC architectures.

***Index Terms*—Global interconnect, hierarchical networks on chip, NoCs, long links design tradeoffs.**

I. Introduction

As the number of modules in System-on-Chip increases, the latency and throughput of pure planar topology NoCs (e.g. 2D mesh) degrade due to the increasing hop distance (number of routers) incurred by long distance (global) packets [1]. Hierarchical schemes [1,2,3,4,5,6] reduce the number of nodes traversed by global packets and therefore provide better scalability. Variable link length is inherent in such topologies and higher hierarchy levels are comprised of longer links. Such long links can reach several millimeters in length. As the RC delay of a link grows rapidly with length [7], RC delays of such links with minimum-size global wires might grow up to many clock cycles.

The approaches to address delays of long links can be divided to three classes: wire sizing and repeaters insertion [8,9,10,11,12]; buffering and pipelining [6], and utilization of techniques such as RF [13], photonic [14] or wave-pipelined fast serial links [15]. Solutions of the third class require radical changes in technology. Although pipelining (class 2) is perceived as a low-cost mainstream approach to cope with excessive delay of combinatorial paths, its utilization in NoC links has two drawbacks. First, pipelining increases the absolute delay of long links since they are divided into N single cycle segments such that $N \cdot T_{Clock} \geq Delay_{Link}$. Second, pipelining incurs excessive buffering and area overheads as extra buffers are needed to compensate for the increased round-trip delay of the flow control mechanism (e.g. credit based, on/off, etc.) among adjacent router ports (Figure 1). Using FIFOs instead of pipelining registers, as proposed in [6], requires larger area compared to pipelining and results in a higher overall link delay. Techniques which reduce the link delay, if possible and cost-effective, are therefore preferable over pipelining. Wire sizing and repeater insertion (class 1) address the source of the problem by decreasing the absolute delay of long wires. In many architectures that comprise long wires [1]– [5] researchers assume that these techniques can be adopted to reduce the delay of long links. Usually, these assumptions are not backed up by a thorough evaluation of the respective costs and the design tradeoffs. In other cases, researchers propose the more complex solutions (i.e. classes 2 and 3) even though wire sizing and repeater insertion could suffice (e.g. [6]).

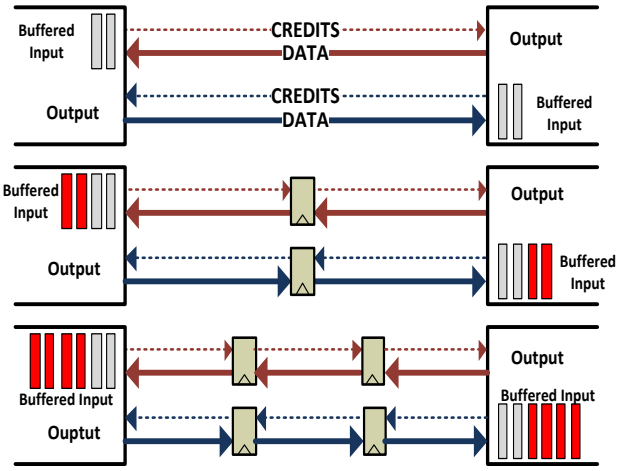

Figure 1. Extra buffering (red bars) due to pipelining of long links.