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Information-Theoretic Sneak-Path Mitigation in Memristor Crossbar Arrays

Yuval Cassuto, *Senior Member, IEEE,*, Shahar Kvatinsky *Student Member, IEEE,*, and Eitan Yaakobi, *Member, IEEE*

Abstract

In a memristor crossbar array, functioning as a memory array, a memristor is positioned on each row-column intersection, and its resistance, low or high, represents two logical states. The state of every memristor can be sensed by the current flowing through the memristor. In this work, we study the sneak path problem in crossbar arrays, in which current can sneak through other cells, resulting in reading a wrong state of the memristor. Our main contributions are modeling the error channel induced by sneak paths, a new characterization of arrays free of sneak paths, and efficient methods to read the array cells while avoiding sneak paths. To each read method we match a constraint on the array content that guarantees sneak-path free readout, and determine the resulting capacity.

Index Terms

Codes for memories, sneak paths, constraint codes, Z channel, memristors, resistive memories, crossbar arrays.

I. Introduction

The memristor technology [14] allows packing storage cells in an unprecedented density, over a simple crossbar structure. The blessing of high storage density and architectural simplicity comes with a major caveat: *data-dependent behavior* [12]. The read accuracy, speed, and power consumption in memristor storage may all vary significantly depending on the instantaneous data stored in the crossbar array. This is clearly an undesired property for a storage medium, and a motivation for data representations that ensure that the physical content of the array corresponds to a well-behaving device. Memristor storage has already motivated a novel data representation for one instantiation of the data-dependence problem [9]. Here we address another very significant data-dependent phenomenon called *sneak paths* [12], causing the read correctness to depend on the array content. The importance of the sneak-path problem can be sensed by the significant body of research addressing it recently in the device and circuit literature [4]–[6], [8], [11], [12], [17], [18].

To understand the sneak-path problem in memristor arrays, we first show a simplified schematic of a memristor array in Fig. 1(a). Each row-column pair is connected by a resistor that can be in either the high-resistance state

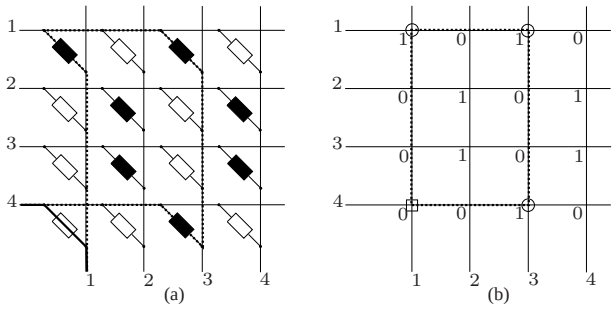

Fig. 1. (a) A memristor array as an array of programmed resistors – white: high resistance, black: low resistance. The high-resistance cell at location $(4, 1)$ has a sneak-path in parallel (plotted dashed), causing it to be read as low-resistance. (b) The corresponding logical values of the memristor array. The cell in the square frame has a sneak-path comprising of the three cells marked in circles.

Yuval Cassuto is with the Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa Israel (email: ycassuto@ee.technion.ac.il).

Shahar Kvatinsky is with the Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa Israel (email: skva@tx.technion.ac.il).

Eitan Yaakobi is with the Department of Computer Science, Technion – Israel Institute of Technology, Haifa Israel (email: yaakobi@cs.technion.ac.il).

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