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Technical Report – Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC)

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***Abstract*-This document describes in detail the optimization problem proposed in [1].**

I. Latency Optimization Problem

The latency optimizing problem of an in-memory Boolean function has two degrees of freedom: the locations of data and the execution time of different logic gates. The following variables are defined for each logic gate:

- $\left(\left\{R_{A_j}, C_{A_j}\right\}, \left\{R_{B_j}, C_{B_j}\right\}, \left\{R_{E_j}, C_{E_j}\right\}\right)$ - Location (coordinates of memory cells) of the inputs and the output of NOR gate *j*.
- $\left(\left\{R_{A_k}, C_{A_k}\right\}, \left\{R_{E_k}, C_{E_k}\right\}\right)$ - Location (coordinates of memory cells) of the inputs and the output of NOT gate *k*.
- T_i - Clock cycle in which gate *i* (either NOT or NOR) is executed.

Therefore, each NOR gate and each NOT gate has 7 and 5 variables, respectively.

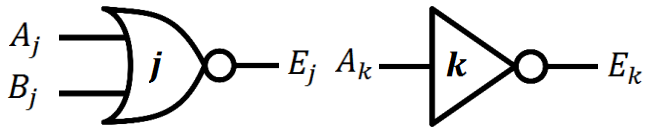

Figure 1 – Inputs and outputs of NOR and NOT gates

The execution of a given Boolean function is finished when the operations of all gates are completed, thus $max_j(T_j)$ is the latency of a specific mapping, where $0 < j \leq \#gates$. Therefore, the latency (in clock cycles) of the best mapping is the minimum latency out of all different mappings and is

$$\boldsymbol{Latency_{best\ mapping} = \min_{0 < j \leq \#gates}\left\{\max_j T_j\right\}}, \quad (1)$$

The legal mappings are limited by location, connectivity and timing, and are restricted by the following constraints:

1) Location constraints:

- Every input and output (I/O) has to be mapped to a memory cell, thus the coordinates of each I/O are limited by the physical size of the memory.

$$\forall \mathbf{x_j} \in \{\mathbf{A_j}, \mathbf{B_j}, \mathbf{E_j}\}: \left(\mathbf{0} < \boldsymbol{C_{x_j}} \leq \boldsymbol{Col_{num}}\right) \cap \left(\mathbf{0} < \boldsymbol{R_{x_j}} \leq \boldsymbol{Row_{num}}\right)$$

- Two different outputs cannot be placed in the same memory cell (whereas the same input may be used for two different gates, therefore their inputs share coordinates). In such a configuration, reusing of a cell (after resetting) is not supported. Note that this constraint is not mandatory and is used to simplify the problem at the cost of potentially using more cells.

$$\forall \boldsymbol{E_k}, \boldsymbol{E_j}: \left(\boldsymbol{C_{E_j}} \neq \boldsymbol{C_{E_k}}\right) \cup \left(\boldsymbol{R_{E_j}} \neq \boldsymbol{R_{E_k}}\right)$$