

Development and Implementation of an FPGA Block on a RISC-V Processor

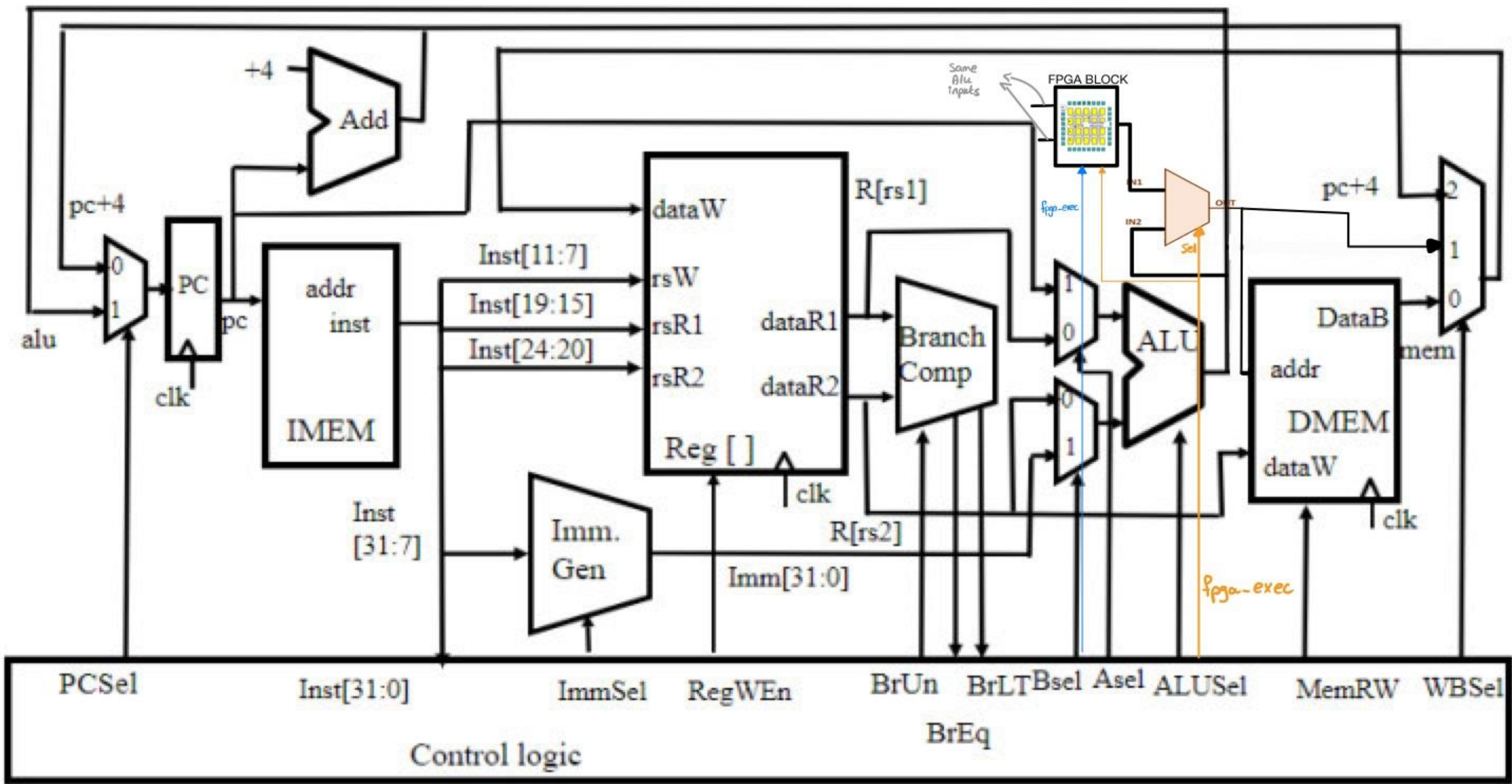
Hala Rabah & Deema khalaily
Supervised by Amnon Stanislavsky



Project description

Designed and integrated a configurable FPGA fabric into a custom single-cycle RISC-V processor. Implemented custom CFG and EXEC instructions for runtime FPGA configuration and execution using SystemVerilog. Verified functionality with modular testbenches, **VCS** simulations, and **Verdi** waveform analysis. Designed the FPGA architecture in draw.io and implemented RTL modules including LUTs, routing, and configuration control. Performed synthesis with **Synopsys Design Vision** and physical design exploration with **Cadence Innovus**. Demonstrated successful integration of FPGA-accelerated operations alongside standard RISC-V ALU execution.

PROCESSOR'S ARCHITECTURE



CFG &

EXEC Operations

CFG Instruction

Opcode 0x7F, funct3=0.
Two CFGs to complete the 62-bit configuration.

1

Configuration Controller

Captures and stores configuration data. cfg_done signals completion before execution.

2

EXEC Instruction

Opcode 0x7F, funct3=1.
Operands are read from the register file.

3

Write-Back Integration

MUX selects ALU or FPGA result. Result written back to register.

4

Synthesis &

Physical Design

RTL to Gates

Synopsys Design Vision Synthesized SV RTL → Gate-level netlist

Physical Design

Cadence Innovus Place & Route flow: floorplan, CTS, routing

FPGA ARCHITECTURE

